User's Guide

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For Safety and Regulatory information,
see the pages behind the index.

Logic Analysis Support for the Motorola MPC826X PowerQUICC II

Solutions for the Motorola MPC826X—At a Glance

The Agilent Technologies E9603A inverse assembler, in conjunction with an Agilent Technologies 16700-series logic analyzer, allows you to view MPC826X PowerQUICC II assembly instructions that are executing in your target system.

The inverse assembler model number is Agilent Technologies E9603A Option 001 when ordered alone. You can also order an analysis probe and inverse assembler, which provides the hardware for easy connection to a target system. The model number for the analysis probe and inverse assembler is Agilent Technologies E9603A Option 002.

The inverse assembler is identified as “Agilent Technologies E8126A” in the Setup Assistant. The analysis probe and inverse assembler is identified as “Agilent Technologies E8125A” in the Setup Assistant.

Additional Equipment Available

Source Correlation Tool Set

The Agilent Technologies B4620B source correlation tool set lets you set up logic analyzer triggers based on source code, and it lets you view the source code associated with signal values captured by the logic analyzer.

In This Book

This book documents the following products:

Product Ordered	Supports	Includes
E9603A Option 001 inverse assembler	MPC8260 MPC8264 MPC8265 MPC8266	The E8126A inverse assembler
E9603A Option 002 analysis probe and inverse assembler	MPC8260 MPC8264 MPC8265 MPC8266	The E8125A analysis probe and inverse assembler and the BGA probing kit (part number E8160-60001)

Tips To Save You Time

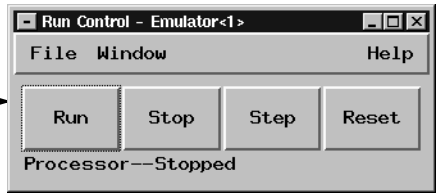
Use the Setup Assistant

Click here to connect the logic analyzer cables, and automatically load the correct configuration files. See page 18.

Use the appropriate Run button

Click here to start a measurement.

If your system includes an emulation probe, click here to run the target microprocessor.



Additional Information Sources

Newer editions of this manual may be available. Contact your local Agilent Technologies representative.

If you have a probing adapter, the instructions for connecting the probe to your target microcontroller are in the **Probing Adapter** documentation.

Application notes may be available from your local Agilent Technologies representative or on the World Wide Web at:

http://www.agilent.com/find/logicanalyzer

The **measurement examples** include valuable tips for making measurements. You can find the measurement examples under the system help in your Agilent Technologies 16700-series logic analysis system.

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1

Equipment and Requirements

This chapter describes:

- Setup Checklist
- Setup Assistant
- Equipment used with the analysis probe and inverse assembler
- List of compatible logic analyzers

Setup Checklist

Follow these steps to connect your equipment:

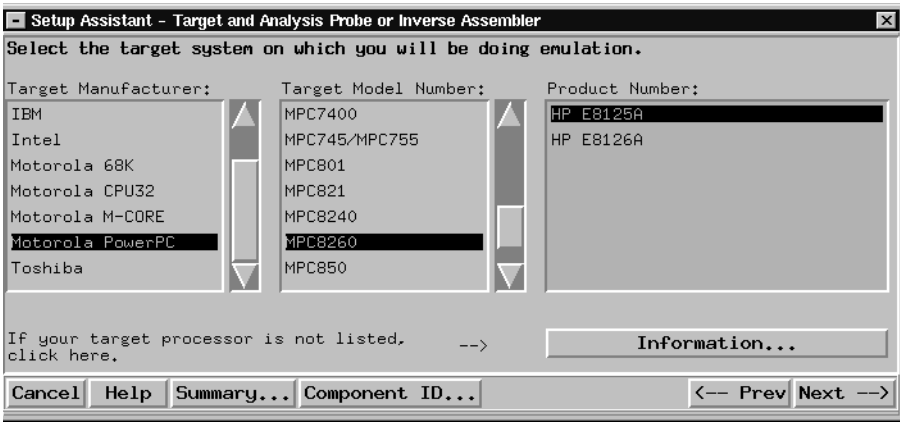
- Check that you received all of the necessary equipment. See page 20.
- Install the software. See page 65.
- Install the analysis probe, if ordered. See page 35. If you have an Agilent Technologies 16700-series logic analysis system, use the Setup Assistant to help you connect and configure your system. See page 18.

Setup Assistant

The Setup Assistant is an on-line tool for connecting and configuring your logic analysis system for microprocessor and bus analysis. The Setup Assistant is available on the 16700-series logic analysis systems. You can use the Setup Assistant in place of the connection and configuration procedures provided in this manual.

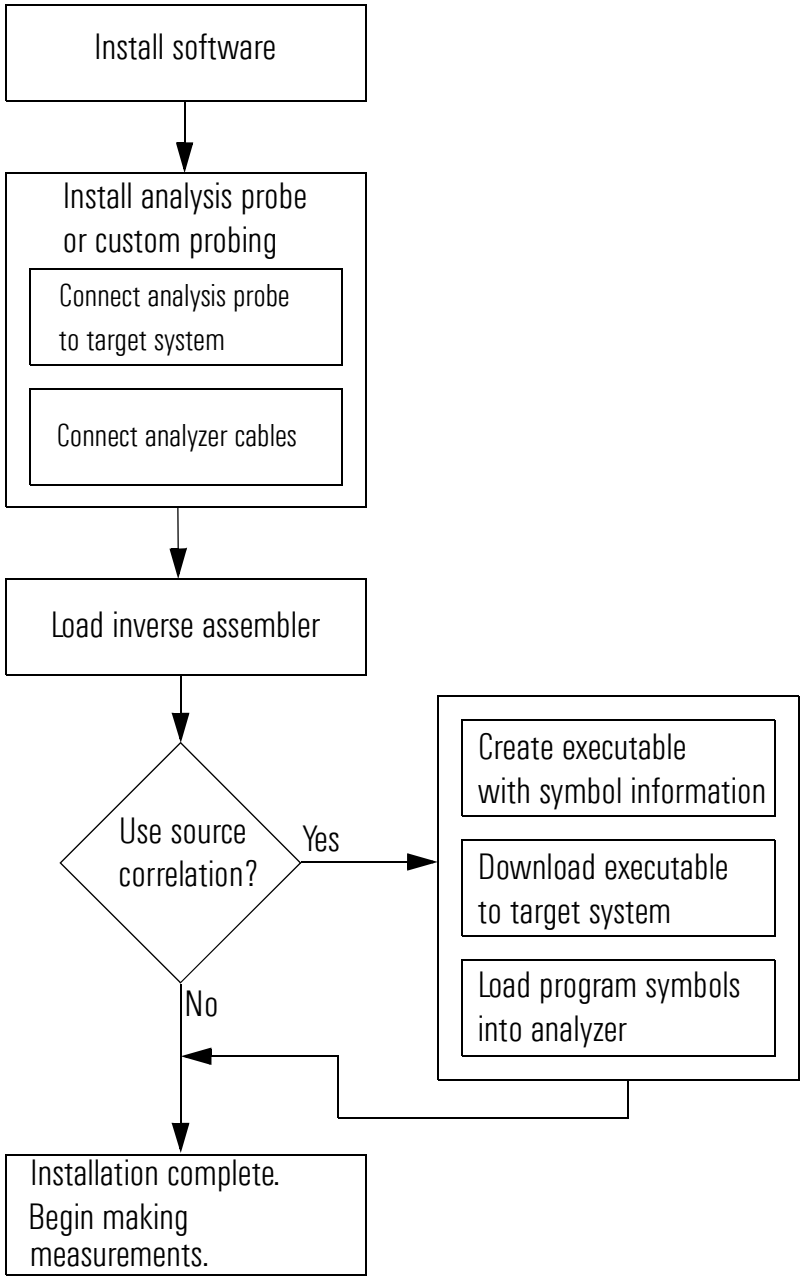
This menu-driven tool will guide you through the connection procedures for connecting the target system to a logic analyzer or other supported equipment. It will also guide you through connecting the logic analyzer to pods on the target system.

Start the Setup Assistant by clicking  in the system window.



If you ordered this product with your Agilent Technologies 16700-series logic analysis system, the logic analysis system has the latest software installed, including support for this product.

- Select E8125A for the inverse assembler when used with an analysis probe
- Select E8126A for the inverse assembler only

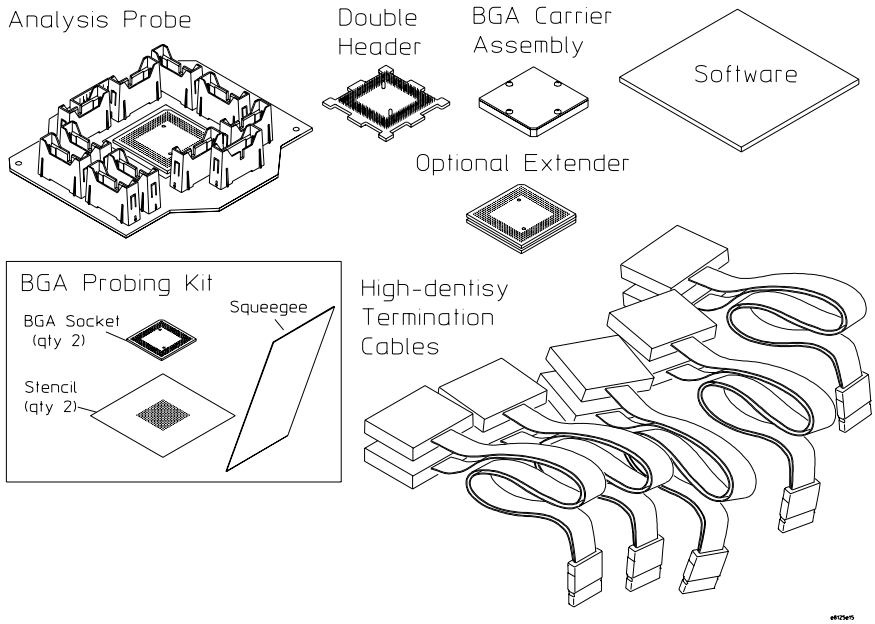

Install software
Install analysis probe or custom probing
Connect analysis probe to target system
Connect analyzer cables
Load inverse assembler
Use source correlation?
Yes
No
Create executable with symbol information
Download executable to target system
Load program symbols into analyzer
Installation complete. Begin making measurements.

Equipment and Software Supplied

Listed below is the equipment and software supplied with:

- The Agilent Technologies E9603A Option 002 analysis probe and inverse assembler.
- The Agilent Technologies E9603A Option 001 inverse assembler.

Analysis Probe



The analysis probe (Agilent Technologies E8125A) includes:

- The Agilent Technologies E8125A analysis probe, which includes a double header, BGA carrier, and optional extender.
- The BGA probing kit (Agilent Technologies part number E8160-60001), which includes installation instructions.
- Five Agilent Technologies E5346A high-density termination cables.
- Logic analyzer configuration files and the inverse assembler software on a CD-ROM (for Agilent Technologies 16700-series logic analysis systems).
- This *User's Guide*.

Inverse Assembler (no Analysis Probe)

The inverse assembler (Agilent Technologies E9603A Option 001 when ordered separately) includes:

- Logic analyzer configuration files and the inverse assembler software on a CD-ROM (for Agilent Technologies 16700-series logic analysis systems).
- This *User's Guide*.

Additional equipment required

In addition to the items listed above, the following is required to analyze an MPC826X PowerQUICC II target system:

- One of the logic analyzers listed in the table on the following page.

If you are using the inverse assembler only (no analysis probe):

- Connector headers on your target system which supply the necessary signals to the logic analyzer.
- Agilent Technologies termination adapter cables to attach your target system to a logic analyzer.

Additional equipment supported

Agilent Technologies B4620B Source Correlation Tool Set.

The analysis probe and inverse assembler may be used with the Agilent Technologies B4620B Source Correlation Tool Set. The software is already installed on the Agilent Technologies 16700-series logic analysis system's disk. All you need is the entitlement certificate for licensing the source correlation tool set software. The CD-ROM is included in case you need to re-install the software.

Compatible Logic Analyzers

A minimum of 136 logic analysis channels (eight logic analyzer pods) are required for inverse assembly. If you choose to probe optional signals, additional logic analyzer pods are required.

The MPC826X PowerQUICC II inverse assembler only works in 16600/700-series logic analysis systems. The 16500 logic analysis system and 166x/167x portable logic analyzer families are not supported.

The inverse assembler works with logic analysis system software version A.02.60 or greater. The latest logic analysis system software version is on the CD-ROM shipped with this emulation solution or inverse assembler product.

Given these restrictions, the following logic analyzers can be used:

Logic Analyzer	Number of Cards	Channel Count
16752A/B	(2 or more cards)	68/card
16751A/B	(2 or more cards)	68/card
16750A/B	(2 or more cards)	68/card
16742A	(2 or more cards)	68/card
16741A	(2 or more cards)	68/card
16740A	(2 or more cards)	68/card
16719A	(2 or more cards)	68/card
16718A	(2 or more cards)	68/card
16717A	(2 or more cards)	68/card
16716A	(2 or more cards)	68/card
16715A	(2 or more cards)	68/card
16712A	(2 cards)	102/card
16711A	(2 cards)	102/card
16710A	(2 cards)	102/card
16601A	n/a	136
16600A	n/a	204
16557D	(1 or 2 cards)	68/card
16556A	(1, 2, or 3 cards)	68/card
16555D/56D	(1, 2, or 3 cards)	68/card
16555A	(1, 2, or 3 cards)	68/card
16554A	(1, 2, or 3 cards)	68/card
16550A	(1 or 2 cards)	102/card

You can use additional logic analyzer cards to monitor additional user-defined signals if desired.

2

Preparing the Target System

There are two ways to probe an MPC826X target system:

- Using an analysis probe.
- Using logic analyzer connectors that have been designed into the target system.

This chapter describes:

- Target system design considerations for logic analysis, which are the same whether you're using an analysis probe or designing connectors into your target system.
- How to attach the analysis probe to your target system.
- Design considerations for including logic analyzer connectors in your target system (when the analysis probe will not be used).

Preparing for Logic Analysis (and Inverse Assembly)

The MPC826X PowerQUICC II inverse assembler for the 16700-series logic analysis system requires a minimum of 136 logic analysis channels (eight pods).

The Motorola MPC8260 VADS evaluation target system requires 152 channels for SDRAM disassembly. If you have two E5346-61605 MICTOR "breakout" pods, you can use flying leads to re-route signals and still use only eight logic analyzer pods.

If optional signals are used, such as PCI analysis, additional logic analyzer pods are required.

You can either use the analysis probe or design high-density connectors into your target system for logic analyzer probe pods.

This section describes these considerations in more detail.

- Design considerations
- Supported PowerQUICC II memory modes
- Attaching the analysis probe to the target system
- Designing logic analyzer connectors into your target system

Design Considerations

There are several things to keep in mind when designing a MPC826X target system.

Configuring for Single Voyager mode vs. 60x Compatibility mode

The MPC826X chip can be configured for either mode. Support for 60x Compatibility Mode can be problematic. Because the MPC826X specification outlines a possible occurrence of a two-stage pipeline, it is important to make sure that this two-stage pipeline can never occur. For complete support of this situation, an analysis probe is required. The inverse assembler does not handle the two-stage pipeline.

Substitution of BAADR[27:31] for ADDR[27:31]

When the BADDR lines are used in place of the ADDR lines, the logic analyzer will be able to trigger on accesses inside of a burst access. Normally, a burst access will broadcast only the starting address for the burst throughout the duration of the burst. This inhibits the logic analyzer from seeing a valid address for each beat of the burst. With the use of the BADDR signals, the full address is shown for each beat of the burst, and the logic analyzer can trigger on those accesses.

The usage of the BADDR signals are only useful in 60x compatibility (multi-master) mode.

Correct multiplexing of status signals

The inverse assembler requires that certain status signals are multiplexed in the proper manner for correct inverse assembly. In particular, the inverse assembler requires the following signal to be multiplexed:

- TC1

Other signals that may be used by the inverse assembler:

- BADDR 29
- BADDR 30
- BADDR 31

Supported PowerQUICC II Memory Modes

This section describes which memory modes the MPC826X inverse assembler supports. Other considerations such as caches and the back-side bus are discussed.

For more chip information, please see Motorola's PowerQUICC II web site:

http://www.mot.com/SPS/PowerPC/

Main memory bus

GPCM/UPM Memory Controllers. The inverse assembler supports the GPCM (General Purpose Chip-select Machine) and UPM (Universal Programmable Machine) in all chip modes.

SDRAM Memory Controller. Support for the SDRAM controller depends upon the revision of the MPC826X processor and the bus mode used.

Single Chip Mode. For MPC826X systems using SDRAM in single-chip mode, there are problems with the debugging bus. The 32-bit address is presented over multiple states, requiring multi-stage acquisition. In this case, more information must be entered in order for the inverse assembler to function properly.

For systems using SDRAM in single-chip mode, the inverse assembler will function correctly if the Enable Bus Visibility bit is set (see “Enabling Full SDRAM Address” on page 34).

60x Compatibility Mode. For systems using SDRAM in 60x compatibility mode, the inverse assembler will function correctly.

Burst Address Modes. The UPM and SDRAM memory controllers have a burst mode. Generally, the BADDR[27:31] signals contain the bursting address. If these signals are unavailable, the inverse assembler will reconstruct the intermediate addresses in software. However, without the physical burst address signals, the logic analyzer is unable to trigger on an intermediate address.

GPCM Memory Controller. This memory controller does not support burst mode.

UPM, Single Chip Mode. The memory controller supports burst mode. The burst address is present on A[27:31] and BADDR[27:31].

UPM, 60x Compatible Mode. The memory controller supports burst mode. The burst address is present only on BADDR[27:31]. Software reconstruction is required if A[27:31] are connected to the logic analyzer.

SDRAM. The memory controller supports burst mode. However, the burst address is never available and requires software reconstruction by the inverse assembler.

Pipelining. Pipelining occurs when the data cycle follows the address cycle. The inverse assembler can handle 0 or 1 stage pipelining without any additional requirements. However, if 2-stage pipelining is present, then an analysis probe must be used.

Single Chip Mode. Two-stage pipelining never occurs.

60x Compatible Mode. Two-stage pipelining is rare, but may occur under certain conditions determined by the memory controller and hardware configuration.

Cache memory

Internal Instruction Cache. The inverse assembler uses branch trace mode. In order to trace in the cache the user must set the MSR.BE bit 22. This BE bit enables a branch trace exception to be taken after a successful completion of a branch instruction. This feature also requires that the data bus is connected and an S-Record executable file is loaded. For additional information on configuring the MSR.BE bit see page 105.

L2 Cache. The inverse assembler will be able to decode line fills to and from an L2 cache connected to the main memory bus. However, line fills are not always analogous to code execution, and they cause unexecuted instructions to be present.

Disabling the instruction cache on the MPC826X

When the instruction cache is enabled, many PowerPC instructions are executed from the cache and do not appear on the external bus. To get an execution trace on the bus, the instruction cache can be disabled. This must be done in supervisor mode. See “Using cache-on trace reconstruction” on page 105.

To disable the cache with the emulation module

Use your debugger or the Emulation Control Interface to configure the HID0 register.

HID0 Register Value	Meaning
0000 8000	Enable Instruction Cache
0000 4000	Enable Data Cache
0000 0800	Invalidate Instruction Cache
0000 0400	Invalidate Data Cache

To disable the cache with code

Disable the instruction cache with the following code:

```
mfspr    r3 hid0
rlwinm   r3 r3 0 17 15 # clear bit 16 (ICE)
mtspr    hid0 r3
isync
```

To also disable the data cache, use:

```
mfspr    r3 hid0
rlwinm   r3 r3 0 18 15 # clear ICE and DCE
mtspr    hid0 r3
isync
```

To invalidate and disable both caches, use:

```
mfspr    r3 hid0
ori      r3 0C00       # set ICFI and DCFI
mtspr    hid0 r3
rlwinm   r3 r3 0 22 19 # clear ICFI and DCFI
mtspr    hid0 r3
rlwinm   r3 r3 0 18 15 # clear ICE and DCE
mtspr    hid0 r3
isync
```

Enabling full SDRAM address

By default, the MPC826X breaks up SDRAM addresses over multiple cycles. In this mode, multiple-level triggers are needed to trigger on SDRAM addresses and the Source Viewer trigger setup commands will not work for code in SDRAM.

For MPC8260 rev. A.1 and higher processors, there is an option that allows the full SDRAM address to be valid on a single state. Enabling this option allows the Source Viewer to trigger correctly on a source line and simplifies manual triggering by eliminating the multiple-level triggers. This mode also increases the speed of the inverse assembler by eliminating the need for time-consuming address reconstruction.

To enable full SDRAM address

To enable the full SDRAM address to be valid on a single state, the Enable Address Visibility (EAV) bit (bit 11 in the Bus Control Register) must be set.

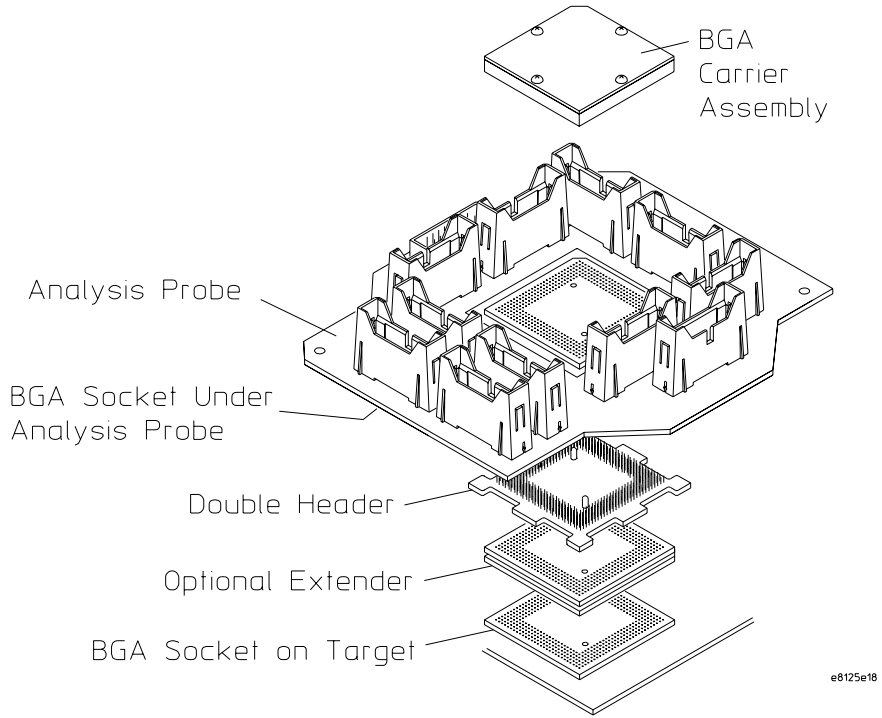
Back-side bus

Local Bus. The local bus is a low latency memory system used for ATM tables and other frequently accessed data structures. The inverse assembler does not support the local bus because these signals are not available from the microprocessor.

PCI Bus. The PCI bus is available in some versions of the PowerQUICC II in place of the local bus. A separate inverse assembler available from FuturePlus Systems or Corelis supports the PCI bus and will disassemble transactions across it. The analysis probe provides connectors compatible with these products.

Attaching the Analysis Probe to the Target System

If you are designing logic analyzer connectors into your target system, and won't be using an analysis probe, skip this section and refer to "Designing Logic Analyzer Connectors into Your Target System" on page 50 instead.



Attaching the E8125A analysis probe to the target system consists of the following steps, which are described on the following pages:

- Set the analysis probe DIP switches.
- Customize the MPC826X SPLL clock filters.
- Customize the JTAG port pullup/pulldown resistors.
- Solder the BGA socket onto the target system.
- Assemble the microprocessor into the BGA carrier.
- Test the target system with the BGA carrier assembly, without the analysis probe.
- Disconnect the BGA carrier assembly from the target system.
- Install the analysis probe onto the target system, and then install the BGA carrier assembly onto the analysis probe.

Protect Your Equipment
The analysis probe socket assembly pins are covered for shipment with a conductive foam wafer or conductive plastic pin protector. This is done to protect the delicate gold-plated pins from damage due to impact. When you're not using the analysis probe, protect the socket assembly pins from damage by covering them with the pin protector.

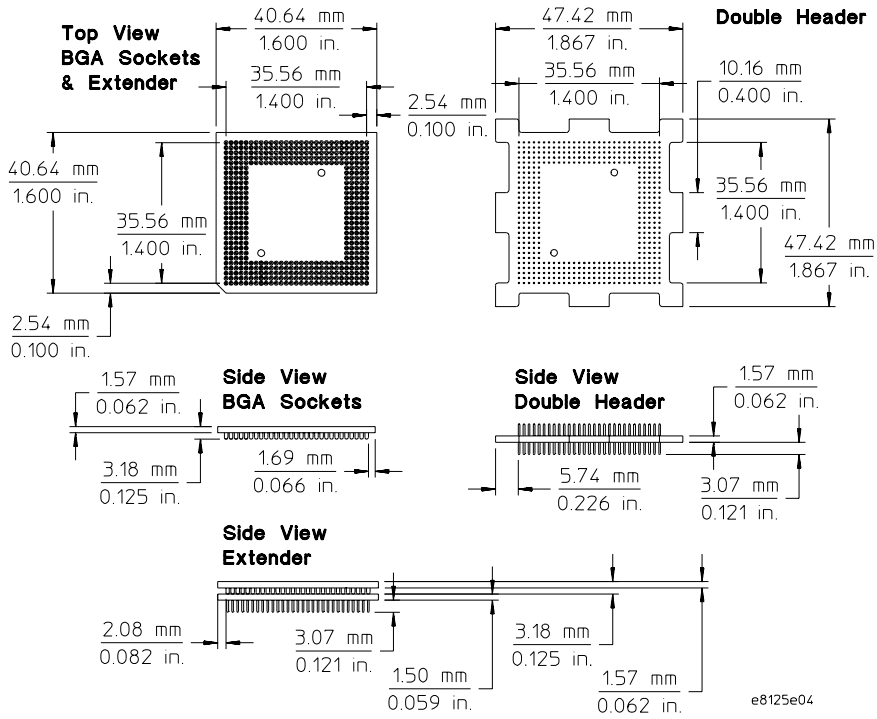
Analysis Probe Considerations

Some things to consider when using the analysis probe are:

- The component keep-out area on the target system.
- The clearance above the target system.
- The analysis probe's dimensions.
- The requirements made by the analysis probe's CLKIN PLL.

Keep-Out Area on Target Board

The analysis probe requires a 47.42 mm by 47.42 mm keep-out area where it overhangs the BGA socket. The maximum height of components under the analysis probe in this area cannot exceed 3.07 mm.



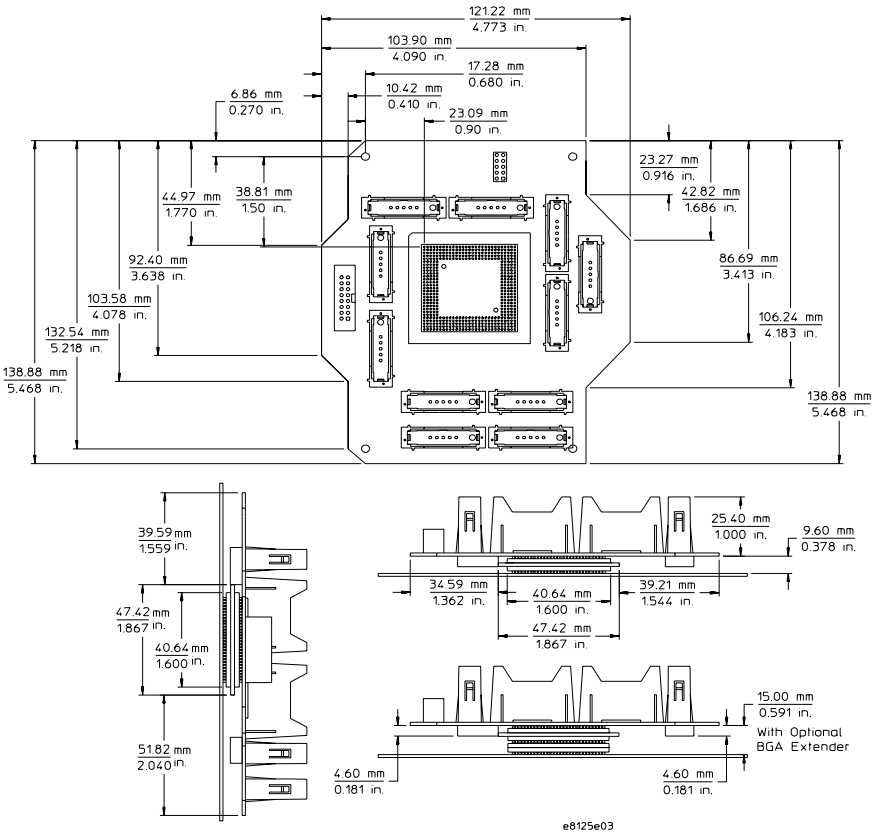
If components are too high for the clearance, order another extender (part number E8125-87607) to add an additional 5.40 mm of clearance. Do not exceed two extenders.

Clearance Above the Target Board

See the diagram on the next page for the dimensions of the analysis probe.

Note that the BGA probing kit will add to the thickness of the analysis probe, for a total of 40 mm. You must also allow space for the cables which plug into the top of the analysis probe.

Analysis Probe Dimensions



Analysis Probe CLKIN PLL Requirements

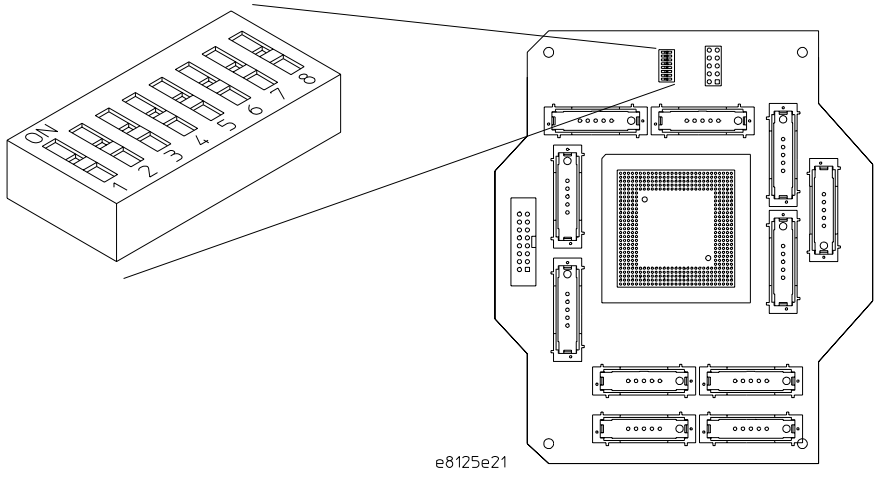
The PLL on the analysis probe that is dedicated to the CLKIN signal has three destinations:

- MICTOR connector J1 Odd Clock (State Clock for the 60X Main Bus)
- MICTOR connector J7 Odd Clock (State Clock for the Local Bus)
- The Altera PLD Clock Input.

The MPC826X target system should be held in reset for 10 msec after CLKIN becomes stable so that the Altera PLD's clock is stable before any bus cycles begin. If this cannot be accomplished for a given target system, asserting HRESET any time after the target system powers up will be adequate for the CLKIN PLL to be stable before any external bus cycles start. (This is assuming that the free-running CLKIN signal is not perturbed during the target system's HRESET sequence.)

Because the CLKIN signal is a free-running clock, without any allowable stops or changes in frequency, the CLKIN PLL should never lose its frequency lock during target system operation.

To set the analysis probe DIP switches

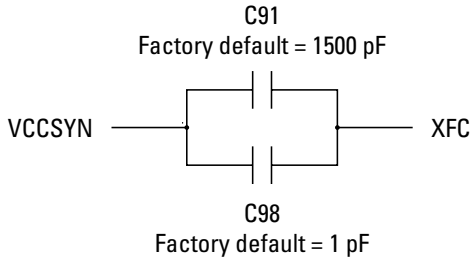


The default position for all switches is OFF.

Switch	Description	OFF	ON
1	JTAG Control	JTAG port is isolated to the analysis probe's JTAG port.	JTAG port is connected to both the analysis probe and the target system's JTAG chain.
2			
3	Address or BADDR signals	MICTOR J1; Odd Data[4:0] represent MPC8260 signals Address[27:31].	MICTOR J1; Odd Data[4:0] represent MPC8260 signals BADDR[27:31].
4			
5	CHECKSTOP Signal Pin	The CHECKSTOP signal comes from MPC8260 Pin D21.	The CHECKSTOP signal comes from MPC8260 Pin R26.
6	Out Of Circuit PLL Operation	All PLLs on the analysis probe are ON.	All PLLs on the analysis probe are OFF.
7	not used		
8	not used		

To customize the MPC826X SPLL clock filters

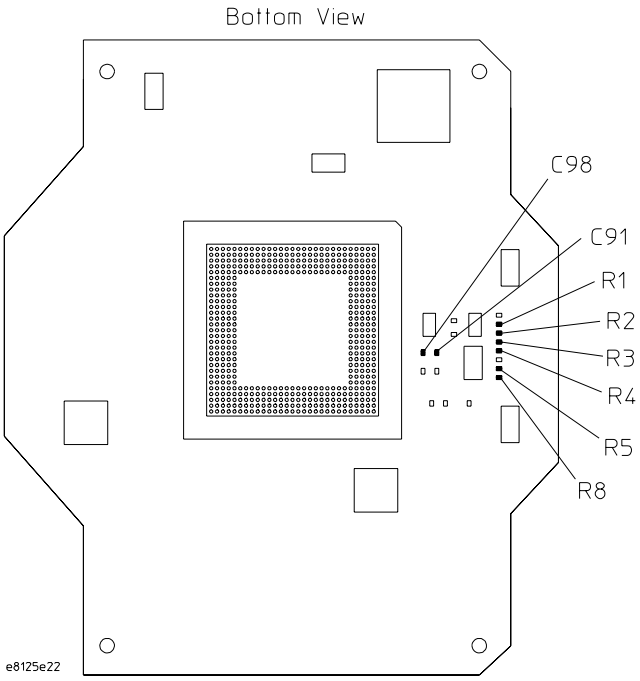
The parallel capacitors C98 and C91 on the analysis probe are provided for customization of the MPC826X SPLL clock filters. These capacitors are connected between XFC and VCCSYN.



The factory-loaded C98 and C91 capacitors are for the Motorola MPC8260 VADS evaluation target system (C98 = 1 pF; C91 = 1500 pF; Ctotal = 1501 pF).

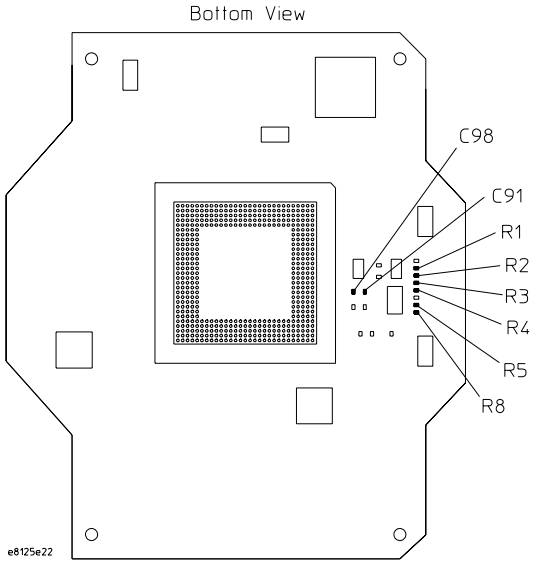
The formulas for determining the correct amount of total capacitance to use between XFC and VCCSYN are outlined in Motorola's *MPC8260 PowerQUICC II User's Manual* under the chapter "Clocks and Power Control."

1 Unsolder and remove the C98 and C91 capacitors that were loaded at the factory.



2 Solder-in the replacement capacitors that are appropriate for your target system.

To customize the JTAG port pullup/pulldown resistors



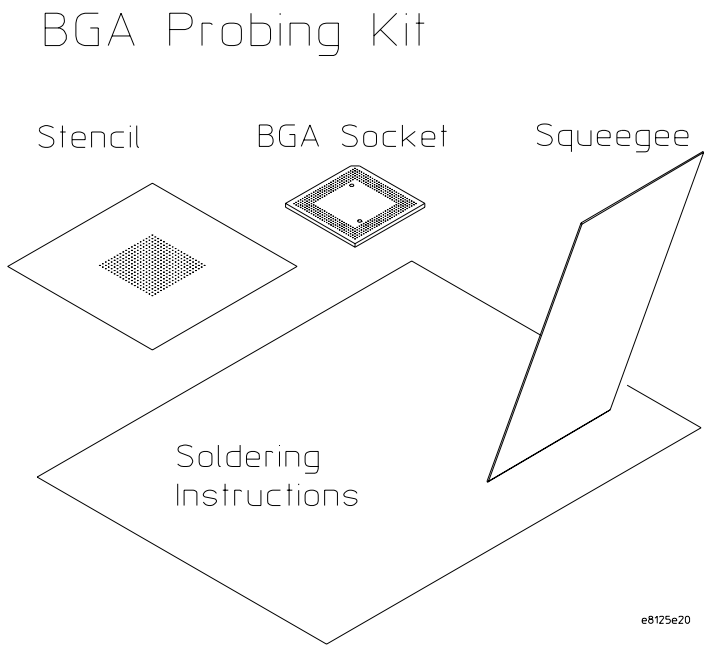
The table on the following page shows the values and circuit locations for resistors R1, R2, R3, R4, R5, and R8. Depending on your target system design, and whether you are routing the JTAG signals to both the JTAG port and the processor, you might want to remove some of these resistors.

Resistor	Analysis Probe DIP Switch	Notes
R1 = 10 k ohm pullup on HRESET R2 = 10 k ohm pullup on SRESET	N/A	The HRESET and SRESET signals on the analysis probe's JTAG port are always connected to the processor and the target system. Depending on the pullup/pulldown resistor values in the target system, R1 and R2 may be removed.
R3 = 10 k ohm pullup on TMS R4 = 10 k ohm pullup on TCK R5 = 10 k ohm pullup on TRST R8 = 1 k ohm pulldown on TDI	S1 = OFF	The analysis probe's JTAG port is connected only to the processor. The R3, R4, R5, and R8 resistors should not be removed in this case.
	S1 = ON	The analysis probe's JTAG port is connected to both the processor and the target system's JTAG chain. Depending on the pullup/pulldown resistor values in the target system, R3, R4, R5, and R8 may be removed.

To solder the BGA socket onto the target system

The BGA probing kit, part number E8160-60001, requires a target system with an empty 480-pin BGA pad array. Install the BGA probing kit using the following instructions.

1. Ensure that your target system has a 480-pin BGA pad array with proper connections for your target microprocessor. This BGA pad array must be clean, unused, and have no solder on its pads.
2. Ensure that pin A1 of the BGA socket is properly aligned with pin A1 on the BGA pad array.
3. Following the soldering instructions in the process sheet that came with the BGA probing kit, install the socket onto the 480-pin BGA pad array, and solder it in place.



To assemble the microprocessor into the BGA carrier

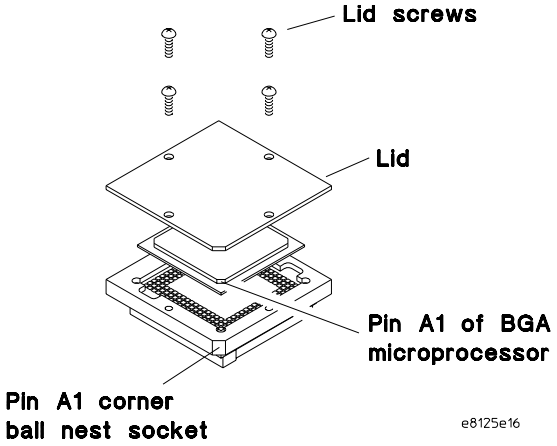
The E8125A analysis probe has a BGA carrier for a 480-pin BGA microprocessor. Use the procedure below to install the BGA microprocessor into the BGA carrier.

1 Align pin A1 on the BGA microprocessor with the pin A1 corner of the BGA carrier (see below).

CAUTION: Serious damage to the target system or analysis probe can result from incorrect connection. Note the position of pin A1 on the BGA carrier and BGA microprocessor prior to making any connection.

2 Place the BGA microprocessor into the BGA carrier, and tighten the lid screws.

Pin A1 Orientation of BGA Microprocessor and BGA Carrier in BGA Carrier Assembly

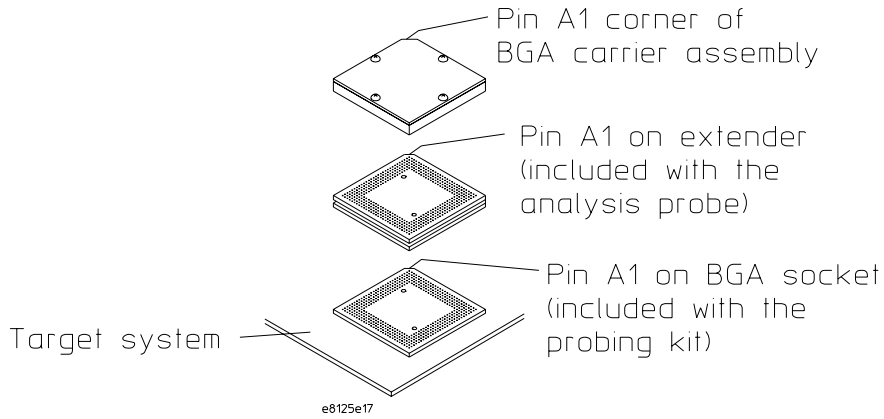


CAUTION: Multiple insertions of the BGA microprocessor into the BGA carrier may degrade the ball nest socket connections. Once the BGA microprocessor is inserted in the ball nest socket, tighten the four lid screws forcefully. Only remove the BGA microprocessor from the BGA carrier when necessary for silicon upgrades.

To test the target system with the BGA carrier assembly

Before installing the analysis probe onto the target system, ensure that the socket and extender have been installed successfully with the following steps.

1. Install the BGA carrier assembly into the extender.
2. Install the extender into the BGA socket on your target system.



3. Turn on your target system and check operation.

   The BGA socket, extender, and BGA carrier assembly add inductance and capacitance. Ensure that your target system operates properly before installing the analysis probe board assembly.

   Open connections or shorts may exist after soldering the BGA socket to the target board. If a previously functioning target board does not function after installing the socket, check continuity of the socket pins. Touch a dry-tip soldering iron to any open pin.

To remove the BGA carrier assembly (or analysis probe) from the socket

You must remove the BGA carrier assembly to attach the analysis probe. Use this procedure when disconnecting the BGA carrier assembly (or the analysis probe) from the BGA socket.

The extractor tool comes with an *Operating Guide* showing how to use the extractor tool to disconnect the BGA carrier assembly or the analysis probe from the BGA socket.

1. Refer to the *Operating Guide* and use the extractor tool to lift the BGA carrier assembly (or the analysis probe) from the socket. Keep all connector pins straight during removal.
2. Do not plug anything other than the analysis probe or optional extender into the BGA socket on the target board.

To attach the analysis probe (with BGA carrier) to the target system

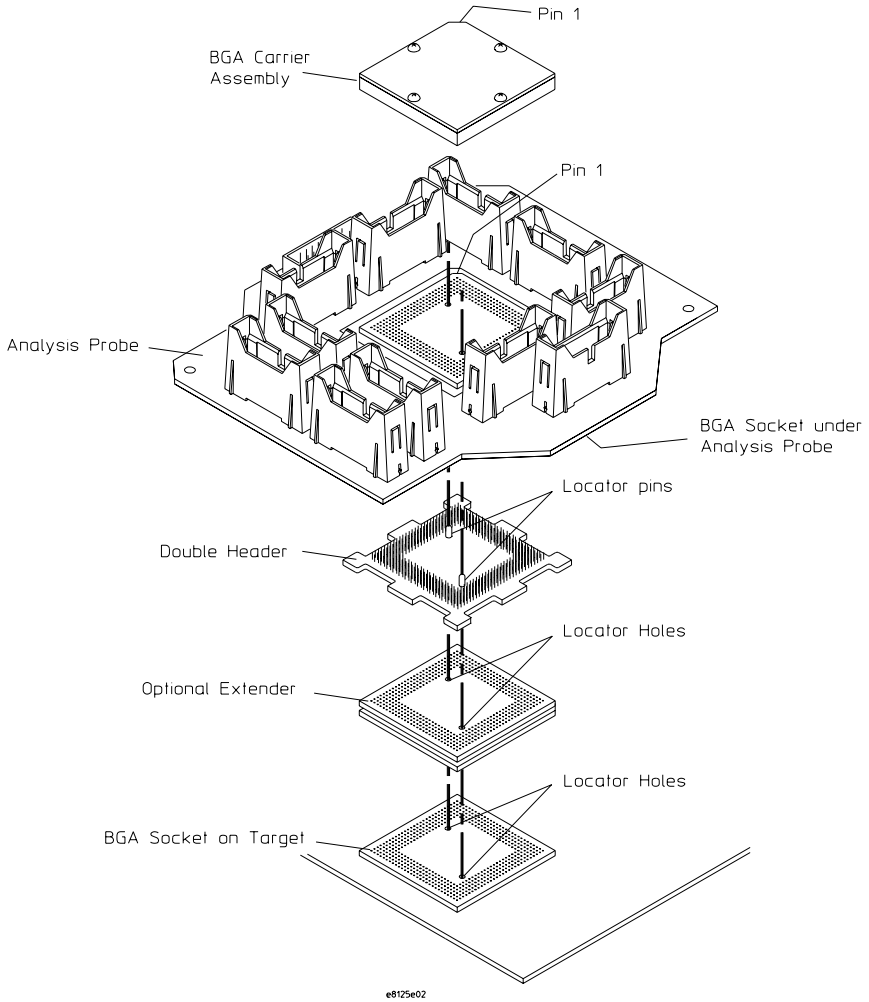
A BGA socket is on the bottom of the analysis probe. It connects to the double header which in turn connects to the extender or socket on the target system.

1. Install the double header into the BGA socket on the bottom of the analysis probe.
2. Install the analysis probe into the extender or socket on the target system. Ensure that pin A1 is properly aligned (see the following figure).

CAUTION: Target System Damage. Serious damage to the target system or analysis probe can result from incorrect connection. Note the position of pin A1 on the target system, double header, analysis probe, and BGA carrier assembly prior to making any connection.

If the analysis probe interferes with components of the target system, or if a higher profile is required, additional BGA extenders (part number E8125-87607) can be used.

Connecting the Analysis Probe to the Target System



Designing Logic Analyzer Connectors into Your Target System

If you are using an analysis probe to make logic analyzer connections to your target system, and won't be designing these connectors into your target system, skip this section and refer to "Attaching the Analysis Probe to the Target System" on page 35 instead.

Using High-Density Connectors

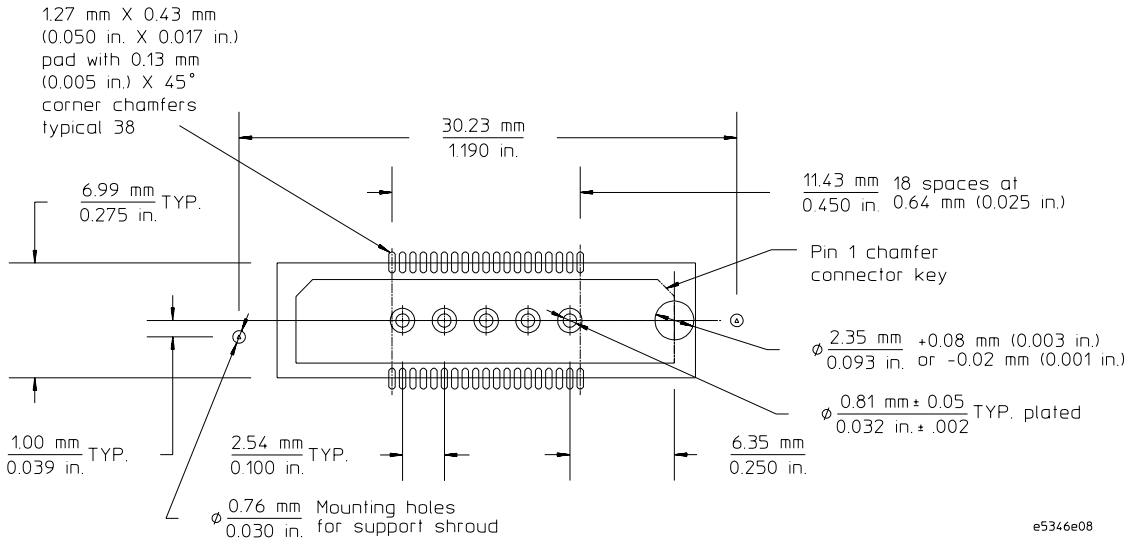
High-density MICTOR (*Matched Impedance ConnecTOR*) connectors are recommended for connecting the target system to the logic analyzer because they require less board space and provide higher signal integrity than medium-density connectors. Each connector carries 32 signals and two clocks.

- Each 32-signal high-density header connector requires approximately 1.1" x 0.4" of printed-circuit board space.
- The part number for the high-density MICTOR connector is: AMP P/N 2-767004-2 or Agilent Technologies: 1252-7431.
- Each MICTOR connector requires one E5346A high-density termination adapter cable to attach to the logic analyzer. This is a Y-cable where the single end connects to the high-density header connector, and each of the two opposite ends connects to a logic analyzer pod.
- Any probed signal line must be able to supply a minimum of 600 mV to the probe tip and handle a minimum loading of 90 k ohms shunted by 10 pF. The maximum input voltage for the logic analyzer is +/- 40 volts peak.
- If a printed-circuit board already has a header connector attached, but the signal pinouts do not match the requirement, an adapter (part number E5346-60002) can be used to route the signals to the correct pods.
- A plastic shroud (part number E5346-44701) is available to secure the mechanical connection of the high-density cable to the MICTOR header connector.

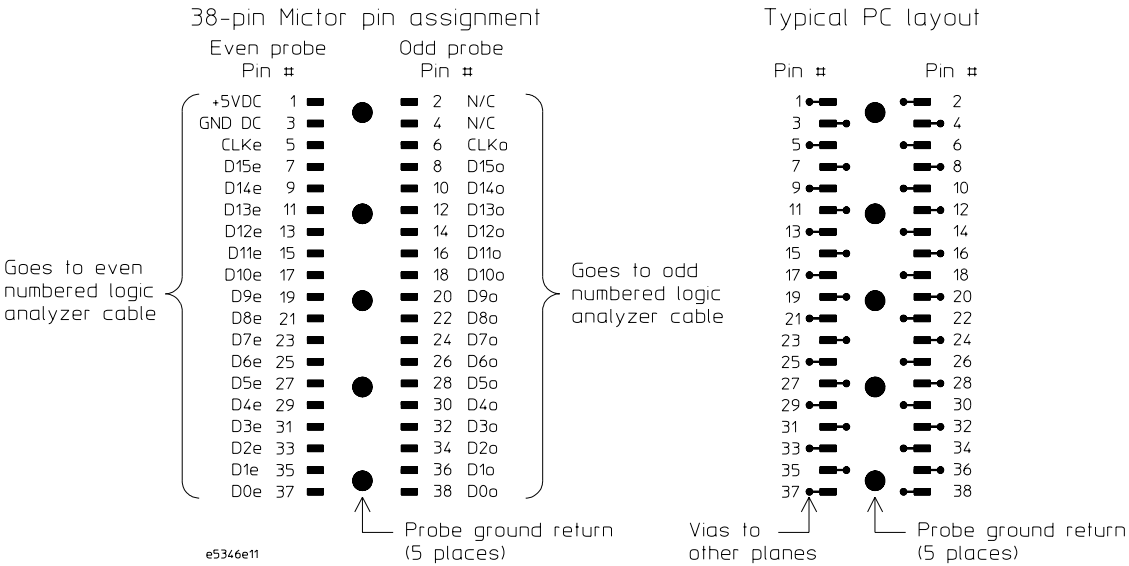
More information on this connector is available by directing your web browser to www.agilent.com and searching for E5346A 38-Pin Probe. Links to additional documents are provided there.

High-Density Connector Mechanical Specifications

Dimensions of the AMP MICTOR 2-767004-2 surface mount connector are shown below. The holes for mounting a support shroud are off-center to allow 0.40 in (1.20 mm) centers when using multiple connectors.



The high-density connector pin assignment and recommended circuit board routing are shown below.



Five center inline pins on the connector are the signal ground returns and must be connected to ground.

Recommended Connector Layout and Signal Routing

The advantages of the recommended configuration are:

- It is optimized for minimum trace lengths and electrical loading.

The disadvantages are:

- It requires five high-density connectors for main memory disassembly in an 8-pod logic analyzer. This is required since pods 7 and 8 are split between two MICTOR connectors to minimize trace lengths.

Recommended Configuration Connection Notes

- “NC” pins MUST be a true no-connect on the target. The signals are used for other functions unavailable to target probing.
- Five center inline pins on the connector are the signal ground returns and must be connected to ground.
- Any blank pins can be used for user defined signals.

- '#' denotes an active low signal.
- J1-J5: Required for Inverse Assembly.
- J6-J7: (Optional) Required for PCI/Local-Bus.
- J8-J11: (Optional) Required for Communications Peripheral visibility.

Motorola MPC8260 VADS Evaluation Target System Routing

The Motorola MPC8260 VADS evaluation target system has a slightly different routing than is specified in the Agilent Technologies recommended configuration. The inverse assembler supports the ADS board in its current configuration. However, Agilent Technologies recommends a slightly different pinout since the Motorola ADS board requires nine logic analyzer pods for (single-chip mode SDRAM) disassembly.

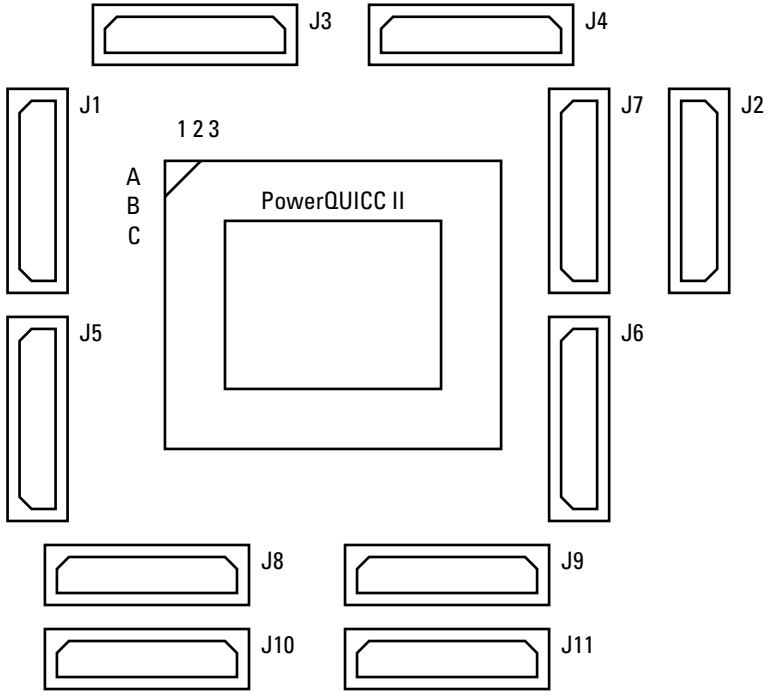
NOTE: Target systems designed to match the Motorola ADS board routing are supported. However, a ninth logic analyzer pod is required for single-chip mode SDRAM disassembly.

The following table describes the differences between the Motorola ADS board routing and the Agilent Technologies recommended pinout.

PowerQUICC II Signal	Recommended	Motorola ADS Board
#PSDRAS	J5 - MICTOR Pin 12	J2 - MICTOR Pin 6

Recommended Connector Layout

The following MICTOR placement is recommended to minimize trace lengths from the BGA to the connectors. Due to the high bus speeds present on the PowerQUICC II, even small trace lengths can affect signal integrity.


J3
J4
J1
J7
J2
1 2 3
A
B
C
PowerQUICC II
J5
J6
J8
J9
J10
J11

Recommended Signal Routing

MICTOR Connector J1				MICTOR Connector J2				MICTOR Connector J3			
Pin	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**
1	NC	2	NC	1	NC	2	NC	1	NC	2	NC
3	NC	4	NC	3	NC	4	NC	3	NC	4	NC
5	#DVAL	6	CLKIN	5	#PSDCAS	6	Reserved	5	#CS2	6	#CS3
7	A0 (MSB)	8	A16	7	#PWE0	8	#PSDWE	7	D32	8	D48
9	A1	10	A17	9	#PWE1	10	PSDA10	9	D33	10	D49
11	A2	12	A18	11	#PWE2	12	#PGTA	11	D34	12	D50
13	A3	14	A19	13	#PWE3	14	PSDAMUX	13	D35	14	D51
15	A4	16	A20	15	#PWE4	16	#BCTL0	15	D36	16	D52
17	A5	18	A21	17	#PWE5	18	DP0	17	D37	18	D53
19	A6	20	A22	19	#PWE6	20	DP1	19	D38	20	D54
21	A7	22	A23	21	#PWE7	22	DP2	21	D39	22	D55
23	A8	24	A24	23	#CS4	24	DP3	23	D40	24	D56
25	A9	26	A25	25	#CS5	26	DP4	25	D41	26	D57
27	A10	28	A26	27	#CS6	28	DP5	27	D42	28	D58
29	A11	30	BADDR27	29	#CS7	30	DP6/CSE0	29	D43	30	D59
31	A12	32	BADDR28	31	#CS8	32	DP7/CSE1	31	D44	32	D60
33	A13	34	BADDR29	33	#CS9	34	Reserved	33	D45	34	D61
35	A14	36	BADDR30	35	#CS10	36	Reserved	35	D46	36	D62
37	A15	38	BADDR31 (LSB)	37	#CS11	38	Reserved	37	D47	38	D63 (LSB)
Even Cable		**Odd Cable**		**Even Cable**		**Odd Cable**		**Even Cable**		**Odd Cable**	
Logic Analyzer Pod 2		**Logic Analyzer Pod 1**		**Logic Analyzer Pod 4**		**Logic Analyzer Pod 9**		**Logic Analyzer Pod 6**		**Logic Analyzer Pod 5**	

Notes:
1. A[27:31] can be used if BADDR[27:31] are unavailable.
2. #PWE[n] is muxed with #PSDQM[n]/#PBS[n].

MICTOR Connector J4				MICTOR Connector J5				MICTOR Connector J6			
Pin	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**
1	NC	2	NC	1	NC	2	NC	1	NC	2	NC
3	NC	4	NC	3	NC	4	NC	3	NC	4	NC
5	#CS0	6	#CS1	5	#TS	6	#AACK	5	#LSDCAS	6	#PCI_CLK
7	D0 (MSB)	8	D16	7	#APE	8	#TBST	7	AD31 (MSB)	8	AD15
9	D1	10	D17	9	#ABB	10	#ARTRY	9	AD30	10	AD14
11	D2	12	D18	11	#BG	12	#PSDRAS/ #POE	11	AD29	12	AD13
13	D3	14	D19	13	#NMI_OUT	14	TSIZ0	13	AD28	14	AD12
15	D4	16	D20	15	#CPU_DBG	16	TSIZ1	15	AD27	16	AD11
17	D5	18	D21	17	#BR	18	TSIZ2	17	AD26	18	AD10
19	D6	20	D22	19	ALE	20	TSIZ3	19	AD25	20	AD9
21	D7	22	D23	21	#DBG	22	TT0	21	AD24	22	AD8
23	D8	24	D24	23	#DBB	24	TT1	23	AD23	24	AD7
25	D9	26	D25	25	TC2	26	TT2	25	AD22	26	AD6
27	D10	28	D26	27	GBL	28	TT3	27	AD21	28	AD5
29	D11	30	D27	29	#L2_HIT	30	TT4	29	AD20	30	AD4
31	D12	32	D28	31	#CPU_BR	32	#TA	31	AD19	32	AD3
33	D13	34	D29	33	#HRESET	34	#TEA	33	AD18	34	AD2
35	D14	36	D30	35	#SRESET	36	TC0	35	AD17	36	AD1
37	D15	38	D31	37	#PORST	38	TC1	37	AD16	38	AD0 (LSB)
Even Cable		**Odd Cable**		**Even Cable**		**Odd Cable**		**Even Cable**		**Odd Cable**	
Logic Analyzer Pod 8		**Logic Analyzer Pod 7**		**Logic Analyzer Pod 10**		**Logic Analyzer Pod 3**		**Logic Analyzer Pod 12**		**Logic Analyzer Pod 11**	

MICTOR Connector J7				MICTOR Connector J8				MICTOR Connector J9			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	NC	2	NC	1	NC	2	NC	1	NC	2	NC
3	NC	4	NC	3	NC	4	NC	3	NC	4	NC
5	#LGTA	6	CLKIN	5	NC	6	NC	5	NC	6	NC
7		8	L_A16/#TRDY	7	PA0	8	PA16	7	PB0	8	PB16
9	LSDAMUX	10	L_A17/#IRDY	9	PA1	10	PA17	9	PB1	10	PB17
11	#LSDAWE	12	L_A18/#STOP	11	PA2	12	PA18	11	PB2	12	PB18
13	LSDA10	14	L_A19/ #DEVSEL	13	PA3	14	PA19	13	PB3	14	PB19
15	#LWR	16	L_A20/ #IDSEL	15	PA4	16	PA20	15	PB4	16	PB20
17	#LSDRAS/ #LOE	18	L_A21/#PERR	17	PA5	18	PA21	17	PB5	18	PB21
19	#LBS0	20	L_A22/#SERR	19	PA6	20	PA22	19	PB6	20	PB22
21	#LBS1	22	L_A23/#REQ0	21	PA7	22	PA23	21	PB7	22	PB23
23	#LBS2	24	L_A24	23	PA8	24	PA24	23	PB8	24	PB24
25	#LBS3	26	L_A25/#GNT0	25	PA9	26	PA25	25	PB9	26	PB25
27	L_DP0	28	L_A26	27	PA10	28	PA26	27	PB10	28	PB26
29	L_DP1	30	L_A27	29	PA11	30	PA27	29	PB11	30	PB27
31	L_DP2	32	L_A28/#RST	31	PA12	32	PA28	31	PB12	32	PB28
33	L_DP3	34	L_A29/#INTA	33	PA13	34	PA29	33	PB13	34	PB29
35	L_A14/ #PAR	36	L_A30/#LOCK	35	PA14	36	PA30	35	PB14	36	PB30
37	L_A15/ #FRAME	38	L_A31	37	PA15	38	PA31	37	PB15	38	PB31
Even Cable		**Odd Cable**		**Even Cable**		**Odd Cable**		**Even Cable**		**Odd Cable**	
Logic Analyzer Pod 14		**Logic Analyzer Pod 13**		**Logic Analyzer Pod 16**		**Logic Analyzer Pod 15**		**Logic Analyzer Pod 18**		**Logic Analyzer Pod 17**	

MICTOR Connector J10				MICTOR Connector J11			
Pin	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**
1	NC	2	NC	1	NC	2	NC
3	NC	4	NC	3	NC	4	NC
5	NC	6	NC	5	NC	6	NC
7	PC0	8	PC16	7	PD0	8	PD16
9	PC1	10	PC17	9	PD1	10	PD17
11	PC2	12	PC18	11	PD2	12	PD18
13	PC3	14	PC19	13	PD3	14	PD19
15	PC4	16	PC20	15	PD4	16	PD20
17	PC5	18	PC21	17	PD5	18	PD21
19	PC6	20	PC22	19	PD6	20	PD22
21	PC7	22	PC23	21	PD7	22	PD23
23	PC8	24	PC24	23	PD8	24	PD24
25	PC9	26	PC25	25	PD9	26	PD25
27	PC10	28	PC26	27	PD10	28	PD26
29	PC11	30	PC27	29	PD11	30	PD27
31	PC12	32	PC28	31	PD12	32	PD28
33	PC13	34	PC29	33	PD13	34	PD29
35	PC14	36	PC30	35	PD14	36	PD30
37	PC15	38	PC31	37	PD15	38	PD31
Even Cable		**Odd Cable**		**Even Cable**		**Odd Cable**	
Logic Analyzer Pod 20		**Logic Analyzer Pod 19**		**Logic Analyzer Pod 22**		**Logic Analyzer Pod 21**	

Alternative Connector Layout and Signal Routing

Agilent Technologies has added an alternative PowerQUICC II pinout which is designed for more efficient use of MICTOR Connectors.

The advantages of the alternative configuration are:

- It requires only four MICTOR connectors for main memory disassembly, versus five connectors in the recommended configuration.
- It provides the same level of main memory disassembly as the recommended configuration in a more compact configuration.

The disadvantages are:

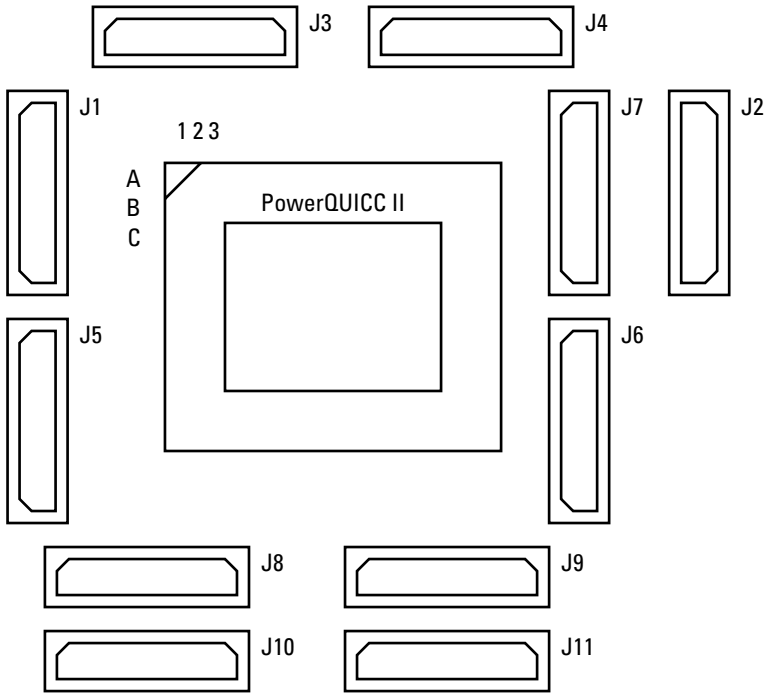
- Requires signals to be routed across the chip, increasing trace lengths and potentially causing signal integrity issues.

Alternative Configuration Connection Notes

- NC pins MUST be a true no-connect on the target. The signals are used for other functions unavailable to target probing.
- Five center inline pins on the connector are the signal ground returns and must be connected to ground.
- Any blank pins can be used for user defined signals.
- J1-J4: Required For Inverse Assembly
- J5: (Optional) Misc. control signals
- J6-J11 minimum configuration routing is identical to the recommended configuration.
- J6-J7: (Optional) Required for PCI/Local Bus
- J8-J11: (Optional) I/O, and Peripherals.

Alternative Connector Layout

The suggested alternative connector layout is the same as the recommended connector layout.



Alternative Signal Routing

MICTOR Connector J1				MICTOR Connector J2				MICTOR Connector J3			
Pin	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**
1	NC	2	NC	1	NC	2	NC	1	NC	2	NC
3	NC	4	NC	3	NC	4	NC	3	NC	4	NC
5	#DVAL	6	CLKIN	5	#PSDCAS	6	#AACK	5	#CS2	6	#CS3
7	A0 (MSB)	8	A16	7	#PWE0	8	#TBST	7	D32	8	D48
9	A1	10	A17	9	#PWE1	10	#ARTRY	9	D33	10	D49
11	A2	12	A18	11	#PWE2	12	#PSDRAS/ #POE	11	D34	12	D50
13	A3	14	A19	13	#PWE3	14	TSIZ0	13	D35	14	D51
15	A4	16	A20	15	#PWE4	16	TSIZ1	15	D36	16	D52
17	A5	18	A21	17	#PWE5	18	TSIZ2	17	D37	18	D53
19	A6	20	A22	19	#PWE6	20	TSIZ3	19	D38	20	D54
21	A7	22	A23	21	#PWE7	22	TT0	21	D39	22	D55
23	A8	24	A24	23	#CS4	24	TT1	23	D40	24	D56
25	A9	26	A25	25	#CS5	26	TT2	25	D41	26	D57
27	A10	28	A26	27	#CS6	28	TT3	27	D42	28	D58
29	A11	30	BADDR27	29	#CS7	30	TT4	29	D43	30	D59
31	A12	32	BADDR28	31	#CS8	32	#TA	31	D44	32	D60
33	A13	34	BADDR29	33	#CS9	34	#TEA	33	D45	34	D61
35	A14	36	BADDR30	35	#CS10	36	TC0	35	D46	36	D62
37	A15	38	BADDR31 (LSB)	37	#CS11	38	TC1	37	D47	38	D63 (LSB)
Even Cable		**Odd Cable**		**Even Cable**		**Odd Cable**		**Even Cable**		**Odd Cable**	
Logic Analyzer Pod 2		**Logic Analyzer Pod 1**		**Logic Analyzer Pod 4**		**Logic Analyzer Pod 3**		**Logic Analyzer Pod 6**		**Logic Analyzer Pod 5**	

Notes:
1. A[27:31] can be used if BADDR[27:31] are unavailable.
2. #PWE[n] is muxed with #PSDQM[n]/#PBS[n].
Shading shows differences from the recommended signal routing.

MICTOR Connector J4				MICTOR Connector J5 (Optional)			
Pin	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**	**Pin**	**MPC8260 Signal**
1	NC	2	NC	1	NC	2	NC
3	NC	4	NC	3	NC	4	NC
5	#CS0	6	#CS1	5	#TS	6	Reserved
7	D0 (MSB)	8	D16	7	#APE	8	#PSDWE
9	D1	10	D17	9	#ABB	10	PSDA10
11	D2	12	D18	11	#BG	12	#PGTA
13	D3	14	D19	13	#NMI_OUT	14	PSDAMUX
15	D4	16	D20	15	#CPU_DBG	16	#BCTL0
17	D5	18	D21	17	#BR	18	DP0
19	D6	20	D22	19	ALE	20	DP1
21	D7	22	D23	21	#DBG	22	DP2
23	D8	24	D24	23	#DBB	24	DP3
25	D9	26	D25	25	TC2	26	DP4
27	D10	28	D26	27	GBL	28	DP5
29	D11	30	D27	29	#L2_HIT	30	DP6/CSE0
31	D12	32	D28	31	#CPU_BR	32	DP7/CSE1
33	D13	34	D29	33	#HRESET	34	Reserved
35	D14	36	D30	35	#SRESET	36	Reserved
37	D15	38	D31	37	#PORST	38	Reserved
Even Cable		**Odd Cable**		**Even Cable**		**Odd Cable**	
Logic Analyzer Pod 8		**Logic Analyzer Pod 7**		**Logic Analyzer Pod 10**		**Logic Analyzer Pod 9**	
Shading shows differences from the recommended signal routing.							

3

Setting Up the Logic Analysis System

Power-ON/Power-OFF Sequence

Listed below are the sequences for powering on and off a fully connected system. Simply stated, your target system is always the last to be powered on, and the first to be powered off.

To power-ON the Agilent Technologies 16700-series logic analysis systems

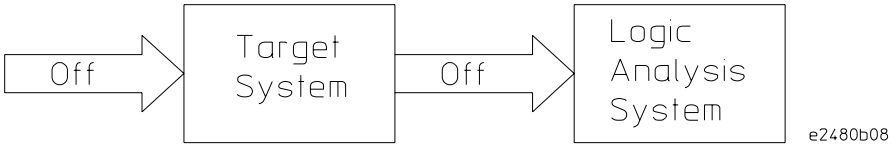
Ensure the target system is powered off.

1. Turn on the logic analyzer. The Setup Assistant will guide you through the process of connecting and configuring the logic analyzer.
2. When the logic analyzer is connected to the target system, and everything is configured, turn on your target system.

To power-OFF

Turn off power to your system in the following order:

1. Turn off your target system.
2. Turn off your logic analysis system.

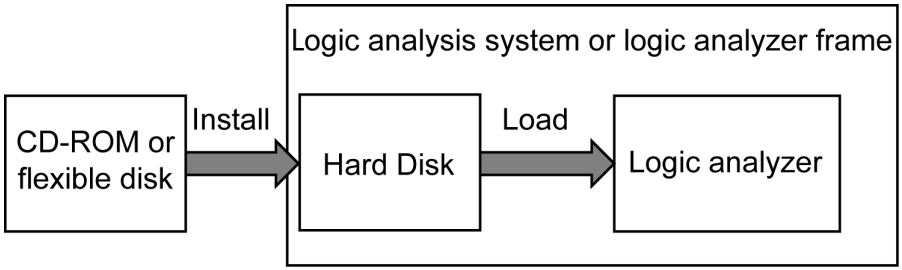


Installing Software

This section explains how to install the software you will need for your inverse assembler.

Installing and loading

Installing the software will copy the files to the hard disk of your logic analysis system. Later, you will need to **load** some of the files into the appropriate measurement module.



What needs to be installed

If you ordered an inverse assembler with your logic analysis system, the software was installed at the factory.

The following files are installed when you install a processor support package from the CD-ROM:

- Logic analysis system configuration files.
- Inverse assembler (automatically loaded with the configuration files).
- Personality files for the Setup Assistant.
- Legacy support for emulation modules

The Agilent Technologies B4620B Source Correlation Tool Set is installed with the logic analysis system's operating system.

To install the software from CD-ROM

Installing a processor support package from a CD-ROM will take just a few minutes. If the processor support package requires an update to the Agilent Technologies 16700 operating system, installation may take approximately 15 minutes.

If the CD-ROM drive is not connected, see the instructions printed on the CD-ROM package.

1. Turn on the CD-ROM drive first and then turn on the logic analysis system.

   If the CD-ROM and analysis system are already turned on, be sure to save any acquired data. The installation process may reboot the logic analysis system.

2. Insert the CD-ROM in the drive.

3. Click the **System Administration** icon. 

4. Click the **Software Install** tab.

5. Click **Install...**.

   Change the media type to "**CD-ROM**" if necessary.

6. Click **Apply**.

7. From the list of types of packages, double-click "**PROC-SUPPORT**."

NOTE: For touch screen systems, double select the "**PROC-SUPPORT**" line by quickly touching it twice.

   A list of the processor support packages on the CD-ROM will be displayed.

8. Click on the "**MPC8260**" package.

   If you are unsure whether this is the correct package, click **Details** for information about the contents of the package.

9. Select **Install**.

   The Continue dialog box will appear.

10. Select **Continue**.

The Software Install dialog will display “Progress: completed successfully” when the installation is complete.

11 If required, the system will automatically reboot. Otherwise, close the software installation windows.

The configuration files are stored in /logic/configs/hp/mpc82xx/mpc8260/. The inverse assemblers are stored in /logic/ia.

See Also

See the instructions printed on the CD-ROM package for a summary of the installation instructions.

See the online help for more information on installing, licensing, and removing software.

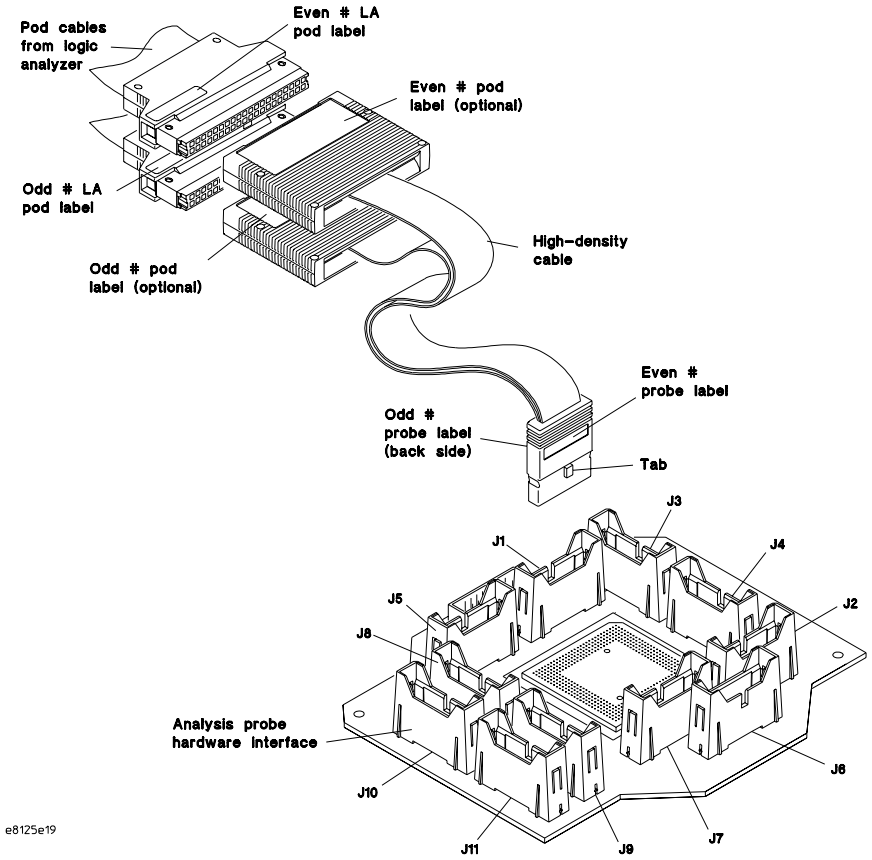
4

Probing the Target System

To connect the high-density termination cables to the analysis probe

Five E5346A high-density termination cables, and labels to identify them, are included with the E8125A analysis probe. Connect the cables to the connectors on the analysis probe as shown in the illustration below. Attach the labels to the cables after connecting the cables to the logic analyzer.

Connecting High-Density Cables to the Analysis Probe



Connecting the Logic Analyzer to the Target System

Each table on the following pages corresponds to a particular logic analyzer. The tables contain connection diagrams for the analysis probe for that logic analyzer. If you are using the inverse assembler only, and have used the recommended signal routing for the headers, these tables will apply to your target system also. You can also use the Setup Assistant to guide you through the connection process. See page 18.

NOTE: If you are using a Motorola ADS board, see "Connecting the Logic Analyzer to the Motorola ADS Target System" on page 78.

CAUTION: Be sure to power down the target system before connecting or disconnecting cables. Otherwise, you may damage circuitry in the analyzer or target system.

The tables are shown in the following order:

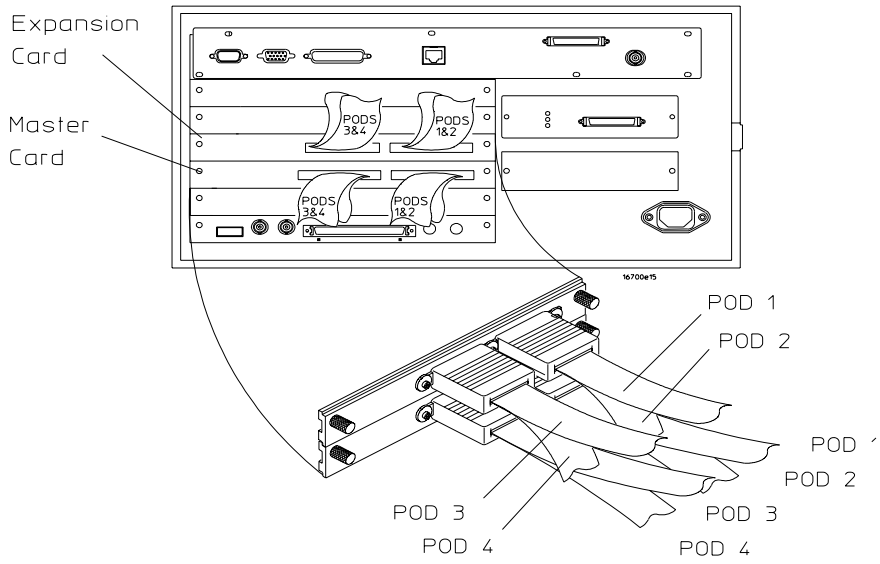
- 16715/16/17/18/19, 16740/41/42, and 16750/51/52 logic analyzers (2 cards). See page 72.
- 16710/11/12A logic analyzers (2 cards). See page 73.
- 16600A logic analyzer. See page 74.
- 16601A logic analyzer. See page 75.
- 16550A logic analyzer (2 cards). See page 76.
- 16554/55/56/57 logic analyzers (2 or 3 cards). See page 77.

Number of Pods Used/Required

The MPC826X inverse assembler requires a minimum of 8 pods. The logic analyzer configuration files assign signals for 12 pods. If fewer than 12 pods are used, only configuration file definitions for the available pods will be used.

NOTE: If you have an Agilent Technologies 16700-series logic analyzer with a logic analyzer card not listed here, use the Setup Assistant to connect and configure your logic analyzer.

To connect a two-card 16715/16/17/18/19, 16740/41/42, or 16750/51/52 logic analyzer

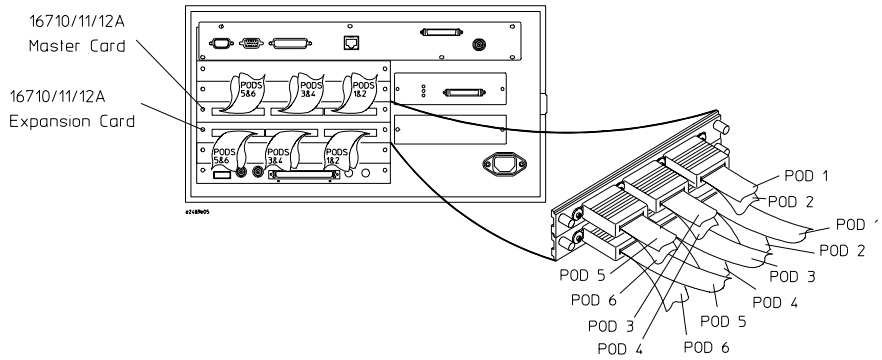


Use this table to connect cables from the two-card 16715/16/17/18/19, 16740/41/42, or 16750/51/52 logic analyzer to the connectors in the target system.

Two-Card 16715/16/17/18/19, 16740/41/42, or 16750/51/52 Logic Analyzer Pod to Connector Mapping

	Pod 4	Pod 3	Pod 2	Pod 1
Expansion Card 1:	J4, Even	J4, Odd	J3, Even	J3, Odd
Master Card:	J2, Even	J5, Odd*	J1, Even	J1, Odd
* When using the alternative signal routing, "J2, Odd" should be connected to this pod.				

To connect a two-card 16710/11/12A logic analyzer

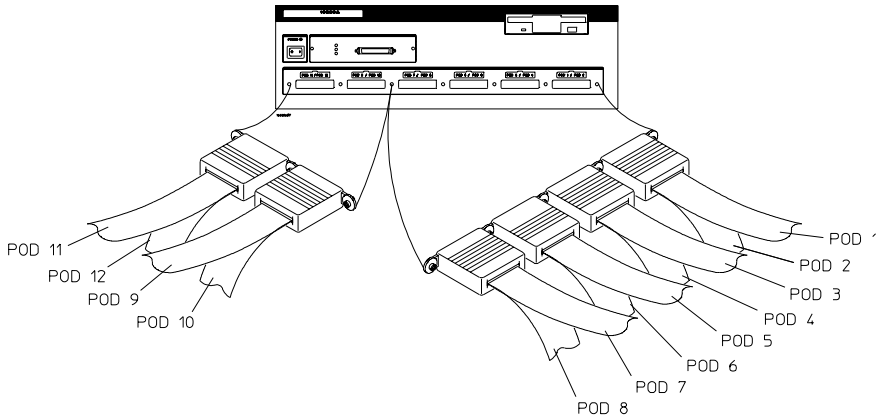


Use this table to connect cables from the 16710/11/12A logic analyzers to the connectors in the target system.

Two-Card 16710/11/12A Logic Analyzer Pod to Connector Mapping

	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Master Card:	J3, Even	J3, Odd	J2, Even	J5, Odd*	J1, Even	J1, Odd
Expansion Card 1:	J6, Even	J6, Odd	J5, Even	J2, Odd*	J4, Even	J4, Odd
* When using the alternative signal routing, these connectors are switched.						

To connect the 16600A logic analyzer



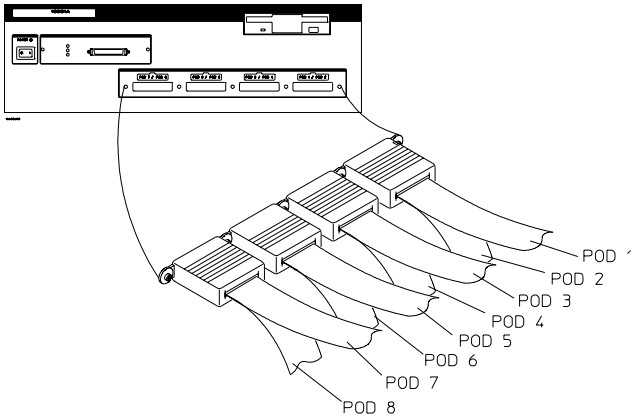
Use this table to connect cables from the 16600A logic analyzer to the connectors in the target system.

16600A Logic Analyzer Pod to Connector Mapping

Pod 12	Pod 11	Pod 10	Pod 9	Pod 8	Pod 7
J6, Even	J6, Odd	J5, Even	J2, Odd*	J4, Even	J4, Odd

Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
J3, Even	J3, Odd	J2, Even	J5, Odd*	J1, Even	J1, Odd
* When using the alternative signal routing, these connectors are switched.					

To connect the 16601A logic analyzer

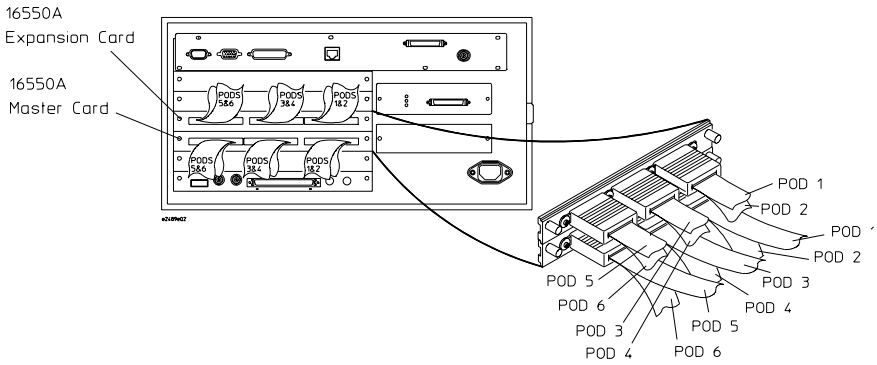


Use this table to connect cables from the 16601A logic analyzer to the connectors in the target system.

16601A Logic Analyzer Pod to Connector Mapping

Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
J4, Even	J4, Odd	J3, Even	J3, Odd	J2, Even	J5, Odd*	J1, Even	J1, Odd
* When using the alternative signal routing, "J2, Odd" should be connected to this pod.							

To connect a two-card 16550A logic analyzer

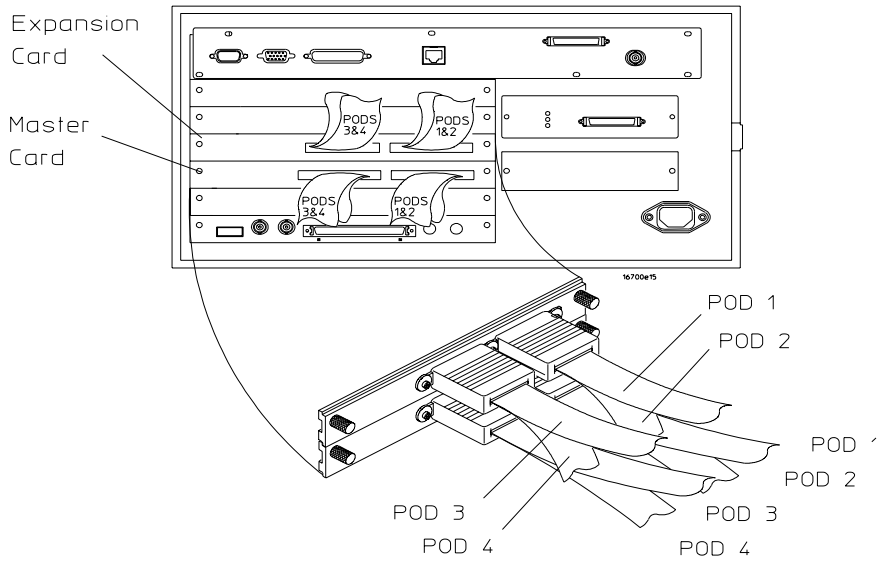


Use this table to connect cables from the 16550A logic analyzer to the connectors in the target system.

Two-Card 16550A Logic Analyzer Pod to Connector Mapping

	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expansion Card 1:	J6, Even	J6, Odd	J5, Even	J2, Odd*	J4, Even	J4, Odd
Master Card:	J3, Even	J3, Odd	J2, Even	J5, Odd*	J1, Even	J1, Odd
* When using the alternative signal routing, these connectors are switched.						

To connect a two-card 16554/55/56/57 logic analyzer



Use this table to connect cables from the two-card 16554/55/56/57 logic analyzer to the connectors in the target system.

Two-Card 16554/55/56/57 Logic Analyzer Pod to Connector Mapping

	Pod 4	Pod 3	Pod 2	Pod 1
Expansion Card 1:	J4, Even	J4, Odd	J3, Even	J3, Odd
Master Card:	J2, Even	J5, Odd*	J1, Even	J1, Odd
* When using the alternative signal routing, “J2, Odd” should be connected to this pod.				

Connecting the Logic Analyzer to the Motorola ADS Target System

The Motorola ADS target system is also known as the MPC8260 VADS evaluation target system.

Each table on the following pages corresponds to a particular logic analyzer. The tables contain connection diagrams for the analysis probe for that logic analyzer. You can also use the Setup Assistant to guide you through the connection process. See page 18.

CAUTION: Be sure to power down the target system before connecting or disconnecting cables. Otherwise, you may damage circuitry in the analyzer or target system.

This section identifies connections to each logic analyzer supported by the inverse assembler. They are shown in the following order:

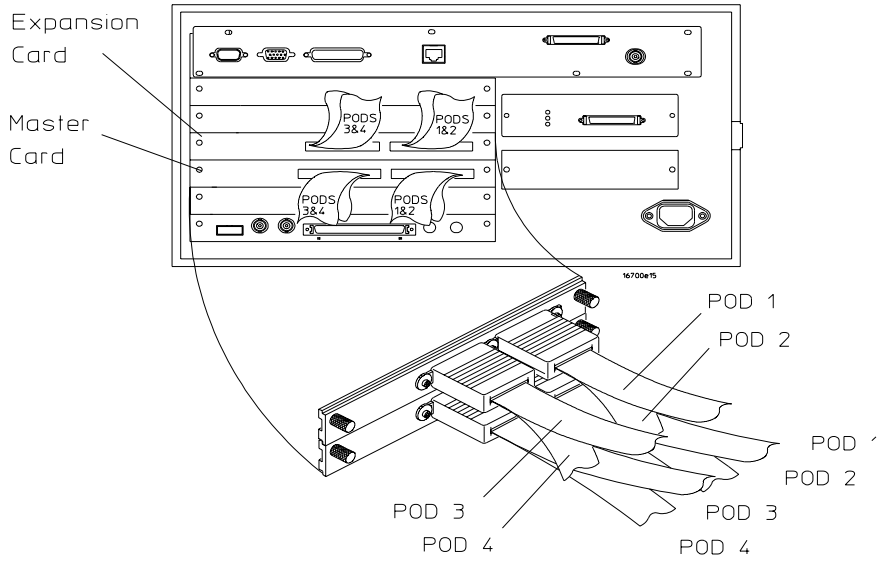
- 16715/16/17/18/19, 16740/41/42, and16750/51/52 logic analyzers (2, 3, 4, or 5 cards). See page 81.
- 16710/11/12A logic analyzers (2 cards). See page 86.
- 16600A logic analyzer. See page 87.
- 16601A logic analyzer. See page 88.
- 16550A logic analyzer (2 cards). See page 90.
- 16554/55/56/57 logic analyzers (2 cards). See page 91.
- 16554/55/56/57 logic analyzers (3 cards). See page 93.
- 16556/57 logic analyzers (4 cards). See page 94.

Number of Pods Used/Required

The MPC826X inverse assembler requires a minimum of 8 pods. The logic analyzer configuration files assign signals for 12 pods. If fewer than 12 pods are used, only configuration file definitions for the available pods will be used.

NOTE: If you have an Agilent Technologies 16700-series logic analyzer with a logic analyzer card not listed here, use the Setup Assistant to connect and configure your logic analyzer.

To connect a two-card 16715/16/17/18/19, 16740/41/42, or 16750/51/52 logic analyzer (ADS)



In order to connect to the Motorola ADS MPC8260 board with only 136 channels, extra hardware is required: Two E5346-60002 high-speed MICTOR adapters and two 01650-61608 16-channel probe lead sets. This extra hardware is required to probe the SDRAS signal on P15(odd) pin number 6. Notice that only 3 MICTOR cables (E5346A) are required for this setup.

Connect the three E5346A high-density probe adapter cables to the P14, P17, and P18 connector headers in the Motorola ADS MPC8260 target system. The ends that connect to the logic analyzer pods are labeled “Odd” and “Even”. Use the following table to connect the Odd/Even E5346A connectors to the logic analyzer pod connectors.

NOTE: The P*xx* numbers in the table correspond to the silk-screened numbers on the Motorola ADS MPC8260 board.

Two-Card 16715/16/17/18/19, 16740/41/42, and 16750/51/52 Logic Analyzer Pod to Motorola ADS Connector Mapping

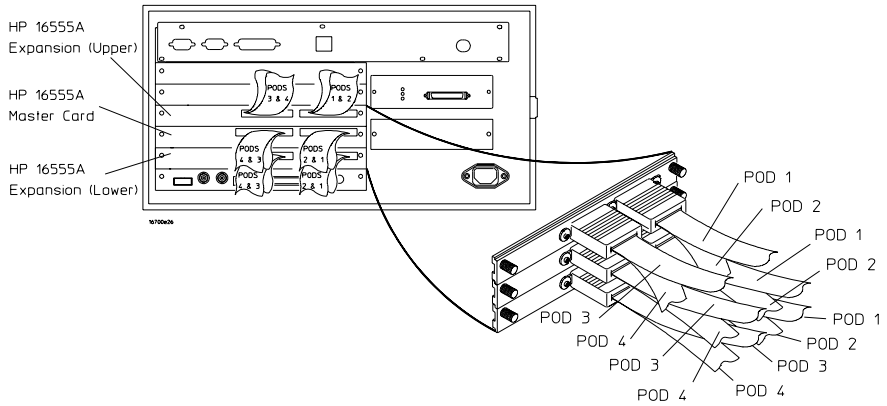
	Pod 4	Pod 3	Pod 2	Pod 1
Expansion Card 1:	P17, Even	P17, Odd	P18, Even	P18, Odd
Master Card:	P15, Even*	P12, Odd*	P14, Even	P14, Odd
* These two pods require the high-speed MICTOR adapter and the two 16-channel probe lead sets.				

Connect the two E5346-60002 MICTOR adapters to P12 and P15 on the target system.

For P12(odd), connect all bits to logic analyzer master pod 3 except logic analyzer bit 13. A connection to P15(odd) pin number 6 should be made here. Leave P12(odd) pin number 12 unconnected.

For P15(even), connect all bits to logic analyzer master pod 4.

To connect a three-card 16715/16/17/18/19, 16740/41/42, or 16750/51/52 logic analyzer (ADS)



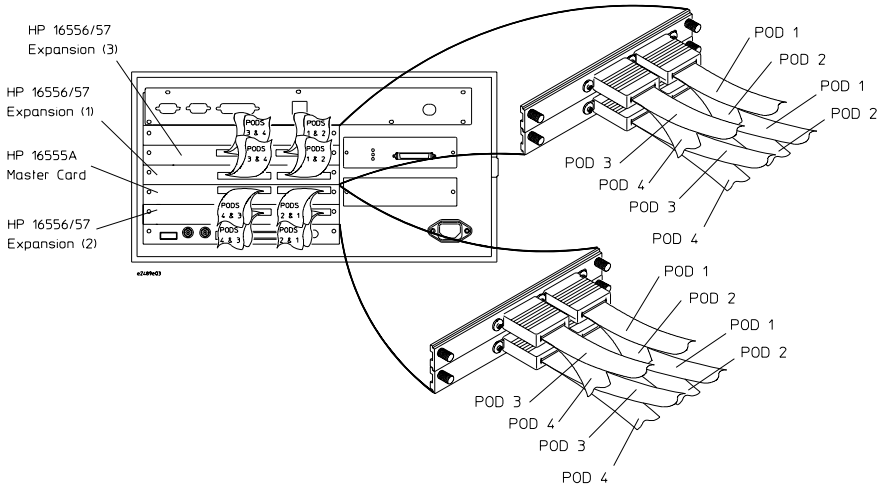
Connect E5346A high-density probe adapter cables (5 required) to each of the connector headers in the Motorola ADS MPC8260 target system. The ends that connect to the logic analyzer pods are labeled "Odd" and "Even". Use the following table to connect the Odd/Even E5346A connectors to the logic analyzer pod connectors.

NOTE: The P*xx* numbers in the table correspond to the silk-screened numbers on the Motorola ADS MPC8260 board.

Three-Card 16715/16/17/18/19, 16740/41/42, or 16750/51/52 Logic Analyzer Pod to Motorola ADS Connector Mapping

	Pod 4	Pod 3	Pod 2	Pod 1
Expansion Card 1:	P17, Even	P17, Odd	P18, Even	P18, Odd
Master Card:	P15, Even	P12, Odd	P14, Even	P14, Odd
Expansion Card 2:	Unused	Unused	P12, Even	P15, Odd

To connect a four-card 16715/16/17/18/19, 16740/41/42, or 16750/51/52 logic analyzer (ADS)



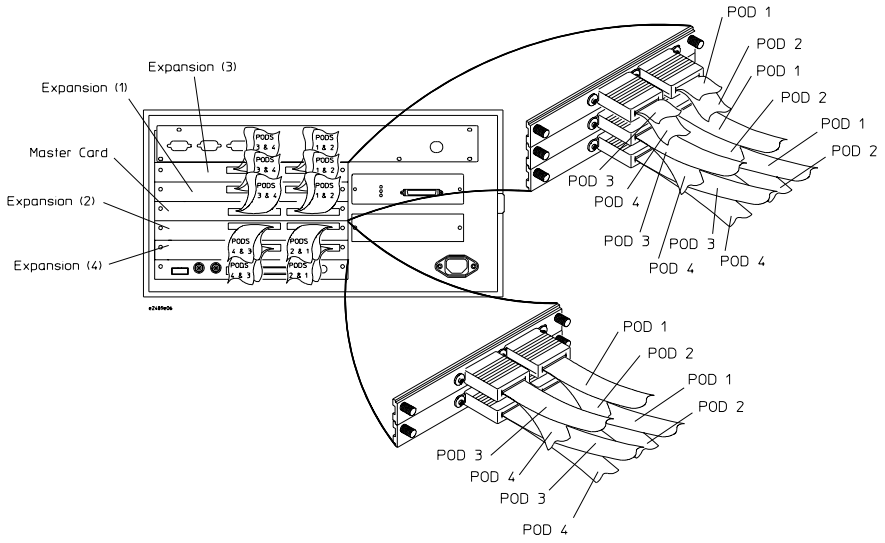
Connect E5346A high-density probe adapter cables (5 required) to each of the connector headers in the Motorola ADS MPC8260 target system. The ends that connect to the logic analyzer pods are labeled “Odd” and “Even”. Use the following table to connect the Odd/Even E5346A connectors to the logic analyzer pod connectors.

NOTE: The P*xx* numbers in the table correspond to the silk-screened numbers on the Motorola ADS MPC8260 board.

Four-Card 16715/16/17/18/19, 16740/41/42, or 16750/51/52 Logic Analyzer Pod to Motorola ADS Connector Mapping

	Pod 4	Pod 3	Pod 2	Pod 1
Expansion Card 3:	Unused	Unused	Unused	Unused
Expansion Card 1:	P17, Even	P17, Odd	P18, Even	P18, Odd
Master Card:	P15, Even	P12, Odd	P14, Even	P14, Odd
Expansion Card 2:	Unused	Unused	P12, Even	P15, Odd

To connect a five-card 16715/16/17/18/19, 16740/41/42, or 16750/51/52 logic analyzer (ADS)



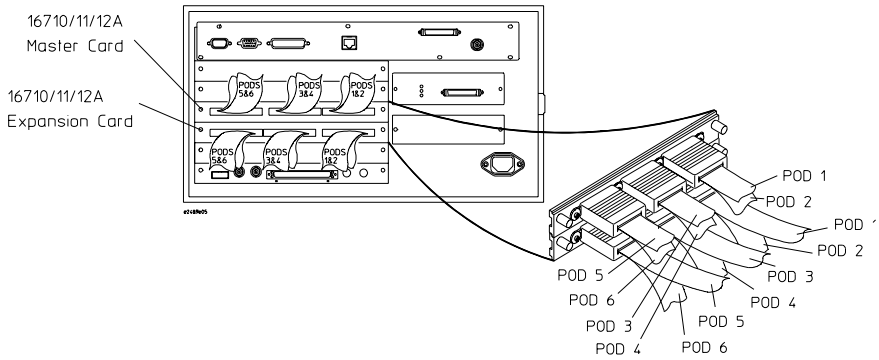
Connect E5346A high-density probe adapter cables (5 required) to each of the connector headers in the Motorola ADS MPC8260 target system. The ends that connect to the logic analyzer pods are labeled “Odd” and “Even”. Use the following table to connect the Odd/Even E5346A connectors to the logic analyzer pod connectors.

NOTE: The P*xx* numbers in the table correspond to the silk-screened numbers on the Motorola ADS MPC8260 board.

Five-Card 16715/16/17/18/19, 16740/41/42, and 16750/51/52 Logic Analyzer Pod to Motorola ADS Connector Mapping

	Pod 4	Pod 3	Pod 2	Pod 1
Expansion Card 3:	Unused	Unused	Unused	Unused
Expansion Card 1:	P17, Even	P17, Odd	P18, Even	P18, Odd
Master Card:	P15, Even	P12, Odd	P14, Even	P14, Odd
Expansion Card 2:	Unused	Unused	P12, Even	P15, Odd
Expansion Card 4:	Unused	Unused	Unused	Unused

To connect a two-card 16710/11/12A logic analyzer (ADS)



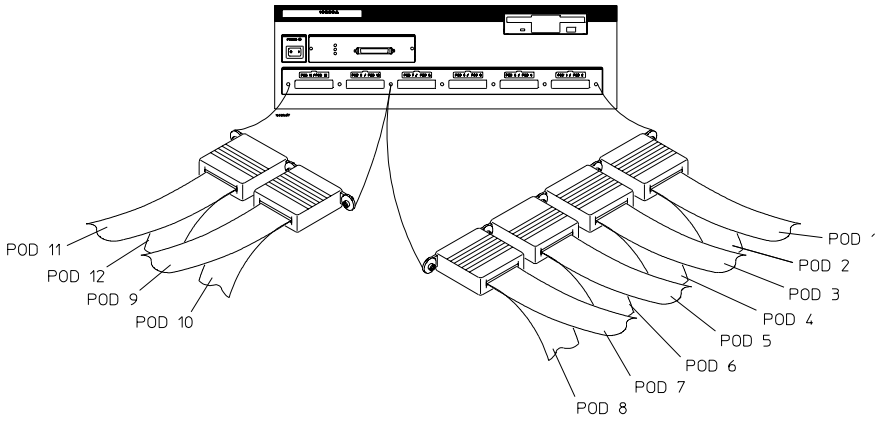
Connect E5346A high-density probe adapter cables (5 required) to each of the connector headers in the Motorola ADS MPC8260 target system. The ends that connect to the logic analyzer pods are labeled "Odd" and "Even". Use the following table to connect the Odd/Even E5346A connectors to the logic analyzer pod connectors.

NOTE: The P*xx* numbers in the table correspond to the silk-screened numbers on the Motorola ADS MPC8260 board.

Two-Card 16710/11/12A Logic Analyzer Pod to Motorola ADS Connector Mapping

	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Master Card:	P18, Even	P18, Odd	P15, Even	P12, Odd	P14, Even	P14, Odd
Expansion Card 1:	Unused	Unused	P12, Even	P15, Odd	P17, Even	P17, Odd

To connect the 16600A logic analyzer (ADS)



Connect E5346A high-density probe adapter cables (5 required) to each of the connector headers in the Motorola ADS MPC8260 target system. The ends that connect to the logic analyzer pods are labeled “Odd” and “Even”. Use the following table to connect the Odd/Even E5346A connectors to the logic analyzer pod connectors.

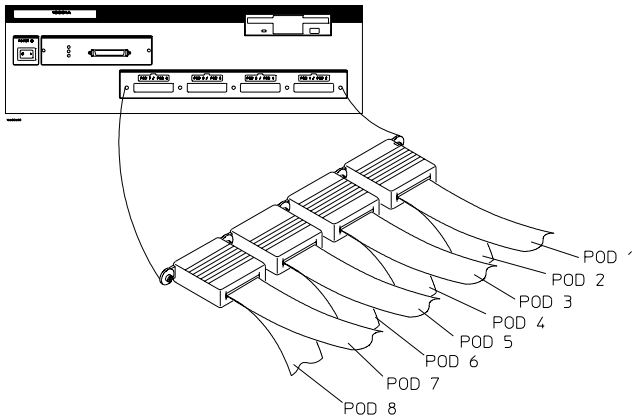
NOTE: The P*xx* numbers in the table correspond to the silk-screened numbers on the Motorola ADS MPC8260 board.

16600A Logic Analyzer Pod to Motorola ADS Connector Mapping

Pod 12	Pod 11	Pod 10	Pod 9	Pod 8	Pod 7
Unused	Unused	P12, Even	P15, Odd	P17, Even	P17, Odd

Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
P18, Even	P18, Odd	P15, Even	P12, Odd	P14, Even	P14, Odd

To connect the 16601A logic analyzer (ADS)



In order to connect to the Motorola ADS MPC8260 board with only 136 channels, extra hardware is required: Two E5346-60002 high-speed MICTOR adapters and two 01650-61608 16-channel probe lead sets. This extra hardware is required to probe the SDRAS signal on P15(odd) pin number 6. Notice that only 3 MICTOR cables (E5346A) are required for this setup.

Connect the three E5346A high-density probe adapter cables to the P14, P17, and P18 connector headers in the Motorola ADS MPC8260 target system. The ends that connect to the logic analyzer pods are labeled “Odd” and “Even”. Use the following table to connect the Odd/Even E5346A connectors to the logic analyzer pod connectors.

NOTE: The P*xx* numbers in the table correspond to the silk-screened numbers on the Motorola ADS MPC8260 board.

16601A Logic Analyzer Pod to Motorola ADS Connector Mapping

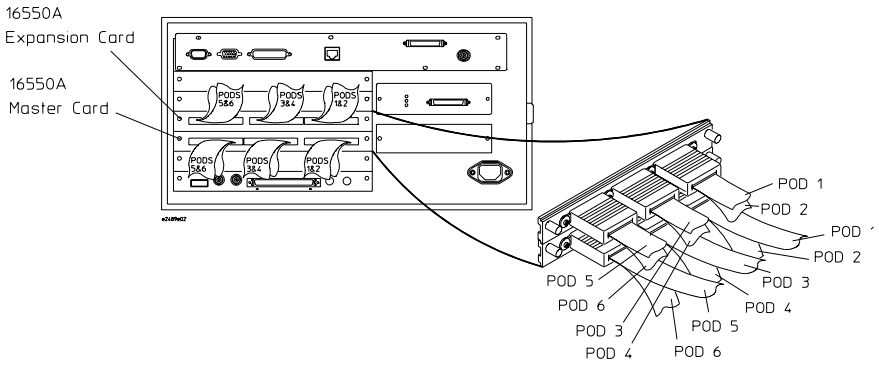
Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
P17, Even	P17, Odd	P18, Even	P18, Odd	P15, Even*	P12, Odd*	P14, Even	P14, Odd
* These two pods require the high-speed MICTOR adapter and the two 16-channel probe lead sets.							

Connect the two E5346-60002 MICTOR adapters to P12 and P15 on the target system.

For P12(odd), connect all bits to logic analyzer master pod 3 except logic analyzer bit 13. A connection to P15(odd) pin number 6 should be made here. Leave P12(odd) pin number 12 unconnected.

For P15(even), connect all bits to logic analyzer master pod 4.

To connect a two-card 16550A logic analyzer



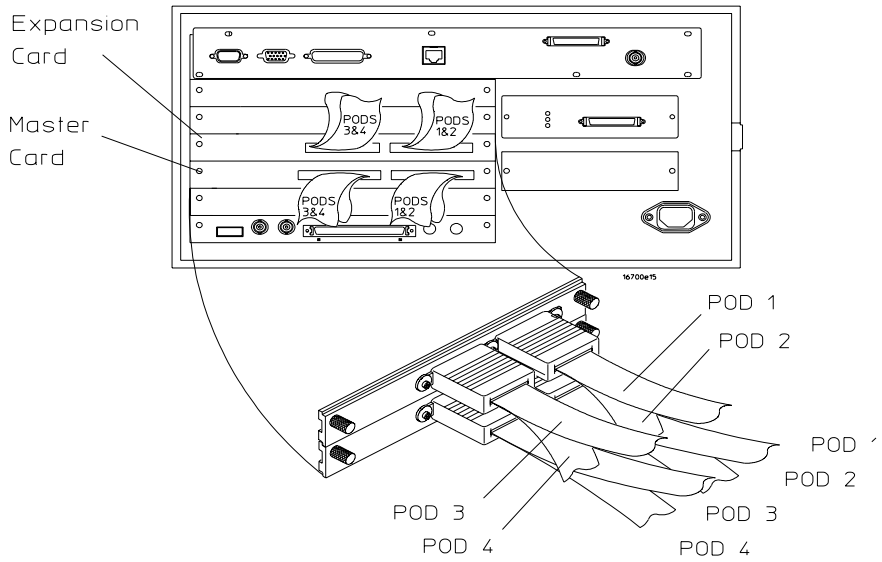
Connect E5346A high-density probe adapter cables (5 required) to each of the connector headers in the Motorola ADS MPC8260 target system. The ends that connect to the logic analyzer pods are labeled “Odd” and “Even”. Use the following table to connect the Odd/Even E5346A connectors to the logic analyzer pod connectors.

NOTE: The P*xx* numbers in the table correspond to the silk-screened numbers on the Motorola ADS MPC8260 board.

Two-Card 16550A Logic Analyzer Pod to Motorola ADS Connector Mapping

	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expansion Card 1:	Unused	Unused	P12, Even	P15, Odd	P17, Even	P17, Odd
Master Card:	P18, Even	P18, Odd	P15, Even	P12, Odd	P14, Even	P14, Odd

To connect a two-card 16554/55/56/57 logic analyzer (ADS)



In order to connect to the Motorola ADS MPC8260 board with only 136 channels, extra hardware is required: Two E5346-60002 high-speed MICTOR adapters and two 01650-61608 16-channel probe lead sets. This extra hardware is required to probe the SDRAS signal on P15(odd) pin number 6. Notice that only 3 MICTOR cables (E5346A) are required for this setup.

Connect the three E5346A high-density probe adapter cables to the P14, P17, and P18 connector headers in the Motorola ADS MPC8260 target system. The ends that connect to the logic analyzer pods are labeled “Odd” and “Even”. Use the following table to connect the Odd/Even E5346A connectors to the logic analyzer pod connectors.

NOTE: The P*xx* numbers in the table correspond to the silk-screened numbers on the Motorola ADS MPC8260 board.

Two-Card 16554/55/56/57 Logic Analyzer Pod to Motorola ADS Connector Mapping

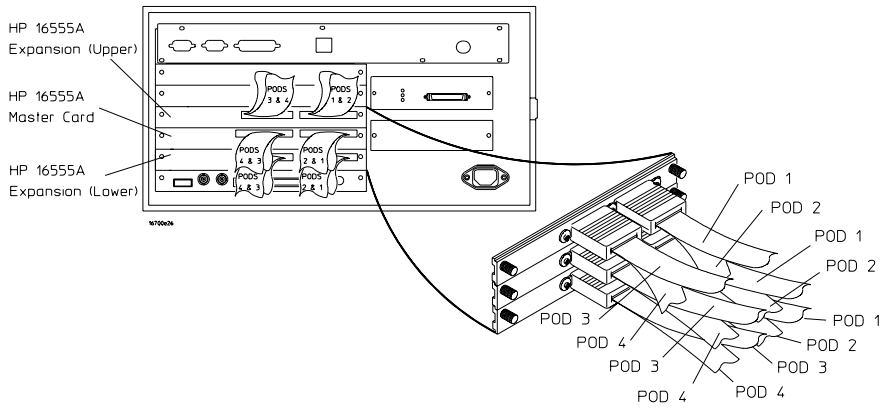
	Pod 4	Pod 3	Pod 2	Pod 1
Expansion Card 1:	P17, Even	P17, Odd	P18, Even	P18, Odd
Master Card:	P15, Even*	P12, Odd*	P14, Even	P14, Odd
* These two pods require the high-speed MICTOR adapter and the two 16-channel probe lead sets.				

Connect the two E5346-60002 MICTOR adapters to P12 and P15 on the target system.

For P12(odd), connect all bits to logic analyzer master pod 3 except logic analyzer bit 13. A connection to P15(odd) pin number 6 should be made here. Leave P12(odd) pin number 12 unconnected.

For P15(even), connect all bits to logic analyzer master pod 4.

To connect a three-card 16554/55/56/57 logic analyzer (ADS)



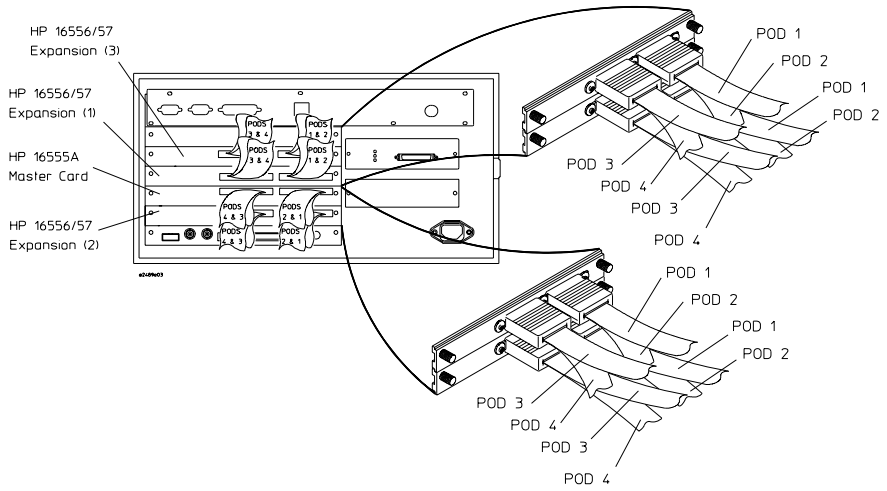
Connect E5346A high-density probe adapter cables (5 required) to each of the connector headers in the Motorola ADS MPC8260 target system. The ends that connect to the logic analyzer pods are labeled “Odd” and “Even”. Use the following table to connect the Odd/Even E5346A connectors to the logic analyzer pod connectors.

NOTE: The P*xx* numbers in the table correspond to the silk-screened numbers on the Motorola ADS MPC8260 board.

Three-Card 16554/55/56/57 Logic Analyzer Pod to Motorola ADS Connector Mapping

	Pod 4	Pod 3	Pod 2	Pod 1
Expansion Card 1:	P17, Even	P17, Odd	P18, Even	P18, Odd
Master Card:	P15, Even	P12, Odd	P14, Even	P14, Odd
Expansion Card 2:	Unused	Unused	P12, Even	P15, Odd

To connect a four-card 16556/57 logic analyzer (ADS)



Connect E5346A high-density probe adapter cables (5 required) to each of the connector headers in the Motorola ADS MPC8260 target system. The ends that connect to the logic analyzer pods are labeled "Odd" and "Even". Use the following table to connect the Odd/Even E5346A connectors to the logic analyzer pod connectors.

NOTE: The P*xx* numbers in the table correspond to the silk-screened numbers on the Motorola ADS MPC8260 board.

Four-Card 16556/57 Logic Analyzer Pod to Motorola ADS Connector Mapping

	Pod 4	Pod 3	Pod 2	Pod 1
Expansion Card 3:	Unused	Unused	Unused	Unused
Expansion Card 1:	P17, Even	P17, Odd	P18, Even	P18, Odd
Master Card:	P15, Even	P12, Odd	P14, Even	P14, Odd
Expansion Card 2:	Unused	Unused	P12, Even	P15, Odd

5

Configuring the Logic Analyzer

The sections of this chapter describe setting up and using the MPC826X inverse assembler. Because your MPC826X target system is designed uniquely according to your needs, it is important that you specify the available signals and memory regions to the inverse assembler.

The information in this chapter is presented in the following sections:

- Loading the configuration file and the inverse assembler
- Tables showing configuration file names
- Using the inverse assembler
- Setting the inverse assembler preferences
- Symbols
- Changing analysis mode

Configuring 16700-series Logic Analysis Systems

You configure the logic analyzer by loading a configuration file. Normally this is done using the Setup Assistant (see page 18). If you did not use the Setup Assistant, you can load the configuration and inverse assembler files from the logic analysis system hard disk.

The information in the configuration file includes:

- Label names and channel assignments for the logic analyzer
- Inverse assembler file name

The configuration file you use is determined by the logic analyzer you are using, and whether you are performing state or timing analysis.

The MPC826X PowerQUICC II inverse assembler decodes captured data into software addresses (SW_ADDR label) and assembly language mnemonics.

To load configuration files (and the inverse assembler) from hard disk

If you use Setup Assistant, it will load configuration files and the inverse assembler for you. This is the preferred method. If you did not use Setup Assistant, you can load the configuration and inverse assembler files from the logic analysis system hard disk.

1 Select the File Manager icon. Use File Manager to ensure that the subdirectory /logic/configs/hp/mpc82xx/mpc8260/ exists.

   If the above directory does not exist, you need to install the MPC8260 Processor Support Package. Close File Manager, then use the procedure on the CD-ROM jacket to install the MPC8260 Processor Support Package before you continue. See “Installing Software” on page 65 for details.

2 Using File Manager, select the configuration file you want to load in the /logic/configs/hp/mpc82xx/mpc8260/ directory, then select **Load**. If you have more than one logic analyzer installed in your logic analysis system, use the Target field to select the machine you want to load.

   The logic analyzer is configured for MPC826X analysis by loading the appropriate MPC8260 configuration file. Loading the indicated file also automatically loads the inverse assembler. The configuration file names are shown in the table on page101.

3 Close File Manager.

To load configuration files (and the inverse assembler) from floppy disk

If you use Setup Assistant, it will load configuration files and the inverse assembler for you. This is the preferred method. If you did not use Setup Assistant, you can load the configuration and inverse assembler files from the logic analysis system hard disk or floppy disk; however, the preferred method is to install this functionality from the CD-ROM onto the hard disk and load from the hard disk.

To install a configuration and inverse assembler file from a floppy disk:

1. Insert the floppy disk in the floppy drive on the Agilent 16700-series logic analysis system mainframe.
2. In the logic analysis System window, select the File Manager icon.
3. In the File Manager window:
   - Set Current Disk to **Flexible Disk**.
   - Set Target to the analyzer you wish to configure.
   - Select the name of the desired configuration file in the Contents frame. The Contents frame lists the configuration files and inverse assembler files available on the floppy disk. These may be either DOS or LIF format files. Either format can be loaded directly into the appropriate logic analyzers.

   Note that the logic analyzers read both DOS and LIF formats. However, only DOS formatted floppy disks can be used to store configurations and data. LIF format floppy disks are read-only.
4. Select **Load**.

   The configuration file you choose will set up the logic analyzer and associated tools. You may see Information, Error, and Warning dialogs that say your configuration has been loaded, and advise you about making proper connections.
5. Select the Workspace window icon to see the arrangement of analysis tools in your configuration.
6. Select the logic analyzer icon in your configuration and choose its **Setup and Trigger...** button to see the way your configuration file defined the Sampling, Format, and Trigger options.

NOTE: Under the **Format** tab, buses are labeled, and bits included in each bus are identified by an asterisk "*".

This procedure restores the configuration that was in effect when the configuration file was saved. Because the file was not saved using your system, you may receive error messages about loading the enhanced inverse assembler or about pods that were truncated. Select the Sampling, Format, and Trigger tabs and modify the configuration to satisfy your measurement desires. Then you can save your customized configuration to DOS format using the File→Save Configuration selection in any of your tool windows, or selecting the Save tab in the File Manager. For details about how to save configuration files, open the Help window.

To list software packages that are installed

- In the System Administration Tools window, select **List...**.

Logic Analyzer Configuration Files

Analyzer Model	Configuration File	Configuration File for Motorola ADS Board
16550A (2 cards)	C8260AP2	C8260AD2
16554A (2 or 3 cards)	C8260AP1 (2 cards) C8260AP3 (3 cards)	C8260AP1 (2 cards) C8260AD3 (3 cards)
16555A/D (2 or 3 cards)	C8260AP1 (2 cards) C8260AP3 (3 cards)	C8260AP1 (2 cards) C8260AD3 (3 cards)
16556A/D (2, 3, or 4 cards)	C8260AP1 (2 cards) C8260AP3 (3 or 4 cards)	C8260AP1 (2 cards) C8260AD3 (3 or 4 cards)
16557D (2, 3, or 4 cards)	C8260AP1 (2 cards) C8260AP3 (3 or 4 cards)	C8260AP1 (2 cards) C8260AD3 (3 or 4 cards)
16600A	C8260AP2	C8260AD2
16601A	C8260AP2	C8260AP1
16710A (2 cards)	C8260AP2	C8260AD2
16711A (2 cards)	C8260AP2	C8260AD2
16712A (2 cards)	C8260AP2	C8260AD2
16715A (2, 3, 4, or 5 cards)	C8260APL1 (2 cards) C8260APL3 (3, 4, or 5 cards)	C8260APL1 (2 cards) C8260ADL3 (3, 4, or 5 cards)
16716A (2, 3, 4, or 5 cards)	C8260APL1 (2 cards) C8260APL3 (3, 4, or 5 cards)	C8260APL1 (2 cards) C8260ADL3 (3, 4, or 5 cards)
16717A (2, 3, 4, or 5 cards)	C8260APL1 (2 cards) C8260APL3 (3, 4, or 5 cards)	C8260APL1 (2 cards) C8260ADL3 (3, 4, or 5 cards)
16718A (2, 3, 4, or 5 cards)	C8260APL1 (2 cards) C8260APL3 (3, 4, or 5 cards)	C8260APL1 (2 cards) C8260ADL3 (3, 4, or 5 cards)

Analyzer Model	Configuration File	Configuration File for Motorola ADS Board
16719A (2, 3, 4, or 5 cards)	C8260APL1 (2 cards) C8260APL3 (3, 4, or 5 cards)	C8260APL1 (2 cards) C8260ADL3 (3, 4, or 5 cards)
16740/41/42A (2, 3, 4, or 5 cards)	C8260APL1 (2 cards) C8260APL3 (3, 4, or 5 cards)	C8260APL1 (2 cards) C8260ADL3 (3, 4, or 5 cards)
16750/51/52A (2, 3, 4, or 5 cards)	C8260APL1 (2 cards) C8260APL3 (3, 4, or 5 cards)	C8260APL1 (2 cards) C8260ADL3 (3, 4, or 5 cards)

The configuration files named C8260AD* are for the Motorola MPC8260 VADS evaluation target system whose signal-to-connector mappings are different than the ones recommended in this manual.

Configuration File Label Descriptions

Label	MPC8260 Signals	Description
AACK	#AACK	Address acknowledge
ABB	#ABB	Address bus busy
ACNT0		Reserved, signal generated by analysis probe
ACNT1		Reserved, signal generated by analysis probe
ADDR	A[0:26], BADDR[27:31]	Address bus, burst address bus
ALE	ALE	Address latch enable
APE	#APE	Address parity error
ARTRY	#ARTRY	Address retry
BCTL0	#BCTL0	Buffer control 0
BG	#BG	Bus grant
BR	#BR	Address bus request
CAS0-7	#PWE[0:7]	Byte select signals used for memory column address strobe
CI	#CI	Cache inhibit
CLKIN	CLKIN	Reference signal (clock input)
CPUBG	#CPU_BG	CPU bus grant

Label	MPC8260 Signals	Description
CPUBR	#CPU_BR	CPU bus request
CPUDBG	#CPU_DBG	CPU bus data bus grant
CS0-11	#CS[0:11]	Chip selects
DATA	D[0:31]	Data bus
DATA_B	D[32:63]	Data bus
DBG	#DBG	Data bus grant
DCNT0		Reserved, signal generated by analysis probe
DCNT1		Reserved, signal generated by analysis probe
DVAL	#DVAL	Data valid
GBL	#GBL	Global
GTA	#PGTA	GPCM transfer acknowledge
HRESET	#HRESET	Hard reset
IRQ6	#IRQ6	Interrupt request
IRQ7	#IRQ7	Interrupt request
L2BG	#EXT_BG2	L2 cache bus grant
L2BR	#EXT_BR2	L2 cache bus request
L2DBG	#EXT_DBG2	L2 cache bus data bus request
L2HIT	#L2_HIT	L2 cache hit
MODCK3	MODCK3	Clock mode input
NMI	#NMI_OUT	Non-maskable interrupt
PORST	#PORESET	Power-on reset
SDCAS	#PSDCAS	SDRAM column address strobe
SDMUX	#PSDAMUX	SDRAM external address multiplexing control
SDRAS	#PSDRAS	SDRAM row address strobe
SDRM10	PSDA10	SDRAM A10 control
SDWE	#PSDWE	SDRAM write enable
SRESET	#SRESET	Soft reset
STAT		Processor control signals
STAT_B		Processor control signals
TA	#TA	Transfer acknowledge
TBST	#TBST	Transfer burst
TC1	TC1	Transfer code

Label	MPC8260 Signals	Description
TEA	#TEA	Transfer error acknowledge
TS	#TS	Transfer start
TSIZ03	TSIZ[0:3]	Transfer size
TT	TT[0:4]	Transfer type
TT RW	TT[1]	Transfer type read/write
VDBB	#DBB	Data bus busy
WT	#WT	Write-through
XBG3	#EXT_BG3	External bus grant 3
XBR3	#EXT_BR3	External bus request 3
XDBG3	#EXT_DBG3	External data bus grant 3

Using the Inverse Assembler

This section discusses the general output format of the inverse assembler and processor-specific information.

Traditional inverse assembly, in which the external processor bus states are captured and decoded, may be implemented by disabling the target's cache. However, this will slow the target significantly, and may induce timing related problems. The target system's performance will be much better if the cache-on trace reconstruction feature is enabled when using the inverse assembler.

Using cache-on trace reconstruction

The inverse assembler uses branch trace mode. In order to trace in the cache you must set the MSR.BE bit 22. This BE bit enables a branch trace exception to be taken after a successful completion of a branch instruction. This feature also requires that the data bus is connected and an S-Record executable file is loaded.

The branch exception is located at 0x00000D00 for an exception prefix MSR.IP=0 or 0xFFF00D00 for an exception prefix MSR.IP=1. The interrupt routine writes the branch target address SRR0 to the tracking address (location in RAM which is non-cached or write-through mode is enabled for that memory block) so that the IA can track the program flow. Also, the tracking address must be on a word boundary.

Example branch exception routine:

```
0x00000d00:  mfspr   r7, d26
0x00000d04:  addis   r8, r0, 0x0000
0x00000d08:  stw     r7, 0x0100(r8)
0x00000d0C:  rfi
```

This branch exception writes the branch target address to a tracking address of 0x00000100.

If you wish to nest interrupts, you must save and restore the SRR0 special purpose register before writing it out to the tracking address. Also, you must write out the exception address at the beginning of the exception.

Example program exception routine:

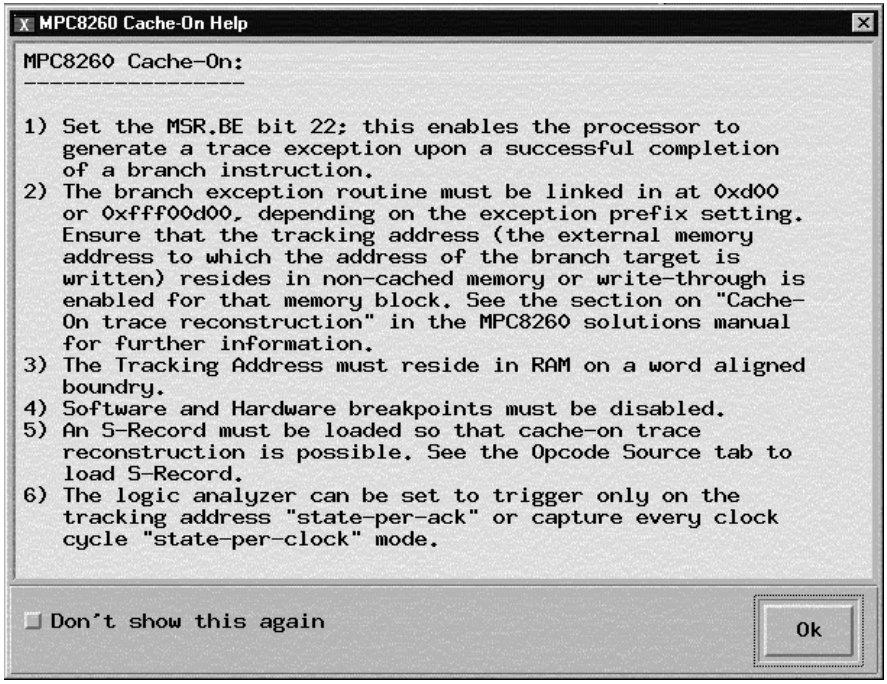
```
0x00000700: addis r6, r0, 0x0000
0x00000704: addi  r6, 0x0700
0x00000708: addis r8, r0, 0x0000
0x0000070C: stw   r6, 0x0100(r8)
0x00000710:  .
0x00000714:  .
0x00000718:  .
0x0000071C: mfspr r7, d26
0x00000720: stw   r7, 0x0100(r8)
0x00000724: rfi
```

To enable cache-on trace reconstruction:

1. Select the **Decoding Options** tab in the Preferences window
2. Set the cache-on mode
3. Set data bus connected
4. Provide the tracking address
5. Select the **Opcode Source** tab
6. Load an S-Record executable file

When cache-on mode is enabled the following dialog will appear.

Cache-on help dialog

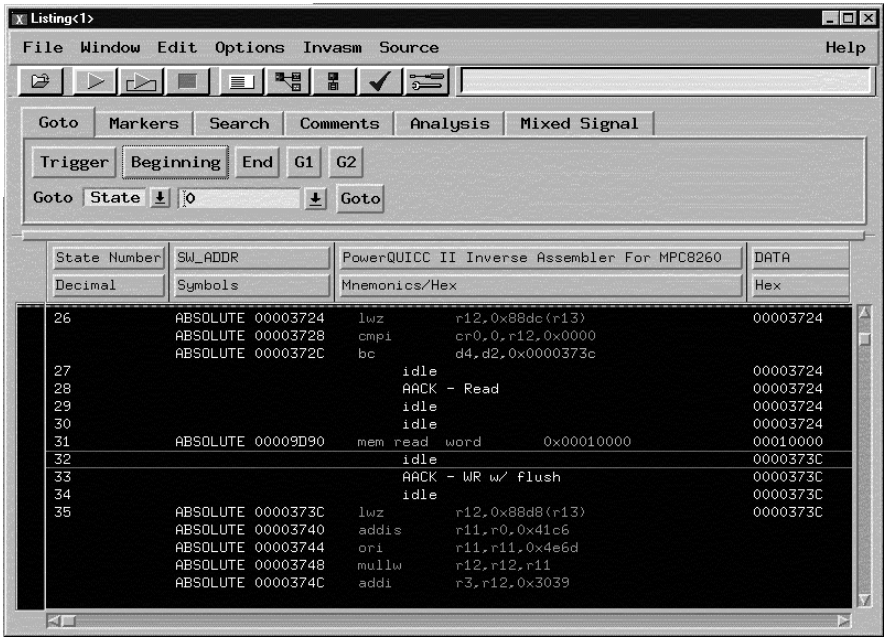


Enabling branch exception disassembly

The following trace shows cache-on execution using branch trace exception disassembly. See page 105 for an explanation of this feature.

To enable branch trace exception, set the MSR.BE bit 22.

Cache-on trace, S-Record executable file loaded, data bus connected, tracking address 0x00001000



Inverse Assembler Modes of Operation

The following table describes the various modes in which the inverse assembler can operate. An explanation of how to set up the inverse assembler to operate in these modes follows.

Inverse Assembler Modes of Operation

IA Cache Decoding	Data Bus Connected	S-Record Loaded	Result
off	no	no	Error message: opcode retrieval requires that the data bus is connected or an S-Record executable file is loaded.
off	no	yes	Opcodes are fetched from the S-Record executable file and decoded into instruction mnemonics. R/W data will not be displayed.
off	yes	no	Traditional Inverse Assembly: Opcodes are fetched from the data bus and decoded into instruction mnemonics. R/W data will be displayed.
off	yes	yes	Opcodes are fetched from the S-Record executable file and decoded into instruction mnemonics. R/W data will be displayed.
on	no	no	Error message: cache-on decoding requires that the data bus is connected and that an S-Record executable file is loaded.
on	no	yes	Error message: cache-on decoding requires that the data bus is connected and that an S-Record executable file is loaded.
on	yes	no	Error message: cache-on decoding requires that the data bus is connected and that an S-Record executable file is loaded.
on	yes	yes	Cache-on Trace Reconstruction: Tracking address data provides the address so opcodes can be fetched from the S-Record executable file and decoded into instruction mnemonics. R/W data will be displayed.

NOTE: Read and write states are always indicated regardless of whether the data bus is connected. When the data bus is connected, read/write data will also be displayed.

To use the Invasm menu

The Invasm menu provides four choices: Load, Preferences, Filter, and Options. Access the Invasm menu in the listing window.

You must use the Preferences dialog to configure the inverse assembler to match the microprocessor memory controller configuration. The other dialogs assist in analyzing and displaying data. The following sections describe these dialogs.

Loading the Inverse Assembler

The Load dialog lets you load a different inverse assembler and apply it to the data in the Listing window. In some cases you may have acquired raw data; you can use the Load dialog to apply an inverse assembler to that data.

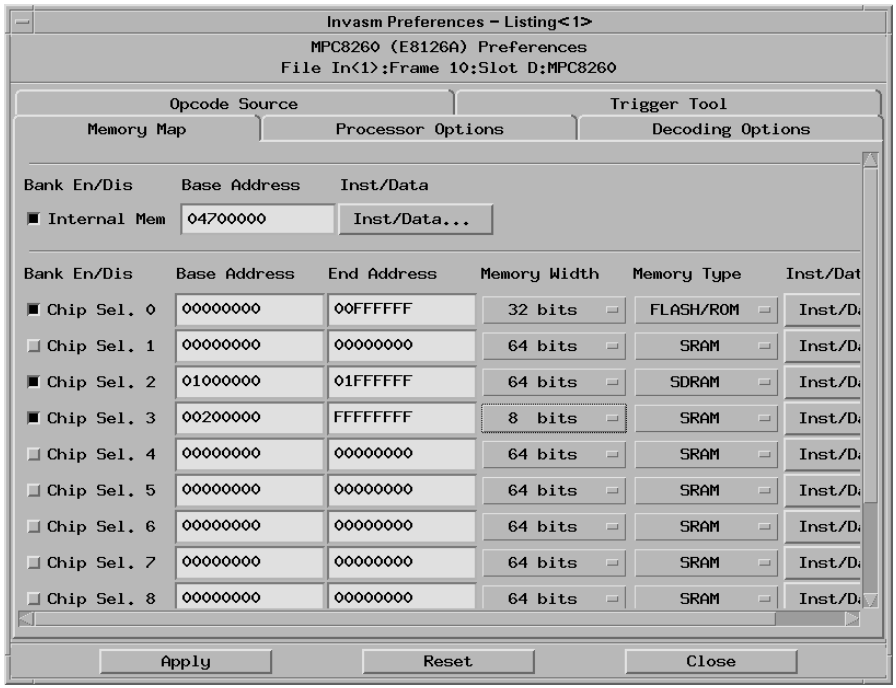
Setting Inverse Assembler Preferences

The inverse assembler Preferences dialog gives the inverse assembler information about your target system so that it can properly disassemble signal values captured by the logic analyzer.

Memory Map

In the MPC826X, the address for a particular cycle will not always be valid at the same time. In fact, depending upon the type of memory that is accessed, there are different signals that assert when a valid address is on the bus. To correctly capture addresses, the inverse assembler must know the memory configuration for your target system.

If a memory bank is allocated to the local bus, leave the chip select disabled since the inverse assembler cannot decode local bus transactions.



Bank Enable/Disable

When the processor is in Single Voyager Mode, the banks MUST be enabled for all of the chip selects that are being used in the system; otherwise, the inverse assembler will not function correctly. These enables are required because chip selects are active low and unconnected logic analyzer channels float low. Without the enables, the inverse assembler could not tell the difference between active and unconnected chip selects.

The enable for internal memory is not used for a chip select. It is used for enabling the inverse assembler to correctly decode internal memory accesses.

Base Address, End Address

Specifies the starting and ending address of the memory bank.

No end address is required for internal memory. The end address is automatically set to the base address plus 128 Kbytes.

Memory Width

Lets you specify an 8-, 16-, 32-, or 64-bit memory width.

Memory Type

Lets you specify a memory type of either SRAM, FLASH/ROM, DRAM, or SDRAM.

Inst/Data Memory Map

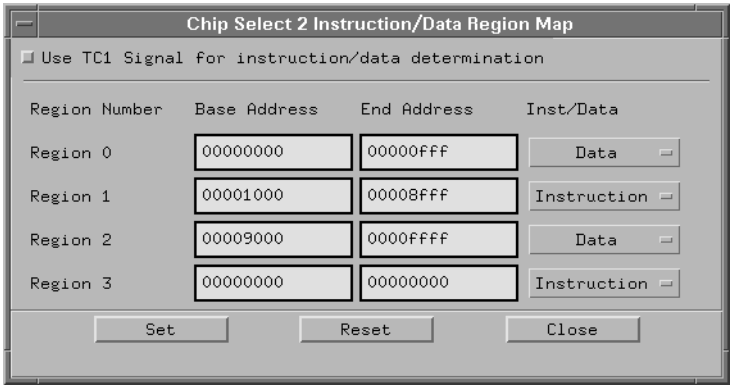
Due to the possible unavailability of the TC1 signal on certain MPC826X targets, the inverse assembler must be able to determine which cycles are instruction and which are data. To solve this problem, the inverse assembler provides a region map for each of the 12 banks of memory that the MPC826X can address plus a region map for internal memory.

The inverse assembler defaults to using TC1 signal. If the target system provides this signal to the inverse assembler, you can ignore the region maps.

You can determine if the target system provides the TC1 signal by looking at the SIUMCR register of the MPC826X. This is a memory-mapped register and the offset from the IMMR is 0x10000. Bits 10 and 11 control the multiplexing of the TC1 signal. If Bits 10 and 11 are 00, TC1 is being provided. If the bits are not 00, TC1 is not being provided.

If your target system does not provide TC1, you must fill out the region maps

for each bank that is enabled. Take care to fill these region maps out correctly because any incorrect entries will cause the inverse assembler to output erroneous data.

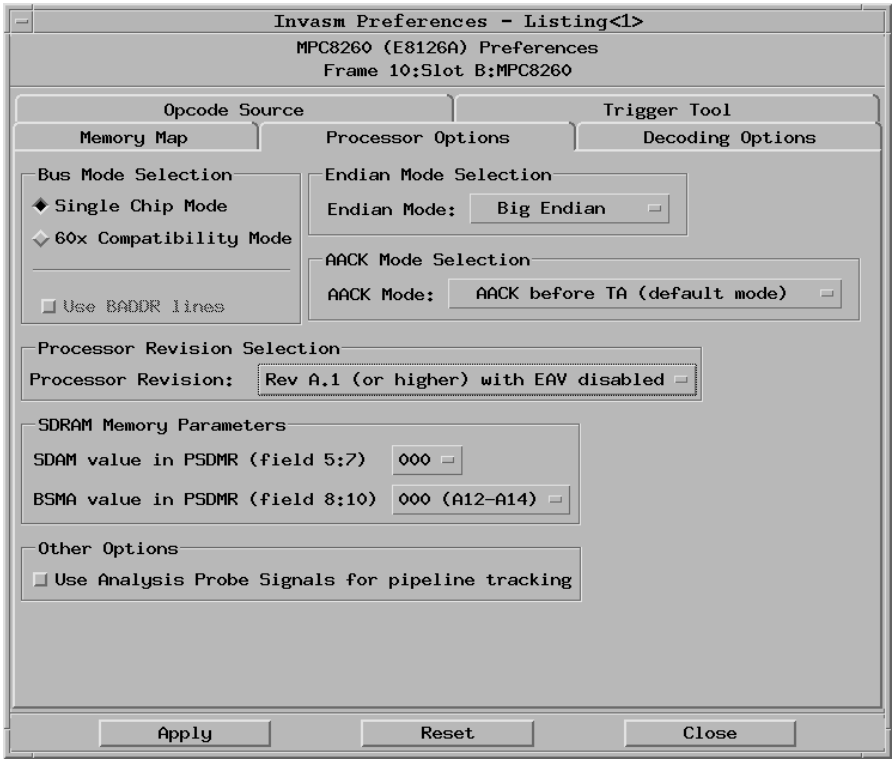


The region maps correspond to the memory map of each individual device that is enabled for that particular chip select. Delineate where code and data lie for each bank that is enabled.

Use TC1 Signal for instruction/data determination. Some target systems do not multiplex TC1 out of the chip. This signal is important for distinguishing between instruction states and data states. If TC1 is unavailable, the inverse assembler will decode all states as instructions.

Processor Options

The Processor Options tab of the Preferences dialog lets you tell the inverse assembler which mode the MPC826X is operating in.



Bus Mode Selection

Single Voyager Mode. In this mode, addresses of transfers are valid on memory dependent signals such as CAS and SDCAS. This mode is intended for systems in which there are no other bus-mastering capable devices.

60x Compatibility Mode. Also known as multi-master mode, this mode is intended for systems that have more than one bus-mastering capable device. A typical configuration would include a MPC826X chip and a PPC750. In this configuration, the 603e processor inside MPC8260 would be disabled and the PPC750 would be the driving processor. In this mode, all addresses are valid at AACK, and no memory dependent signals are required to capture a 32-bit physical address.

Use BADDR lines. This selection tells the inverse assembler to use the BADDR lines for burst addresses. If the BADDR lines are not present, this option should not be selected; that tells the inverse assembler to reconstruct the burst addresses from UPM accesses instead.

Endian Mode Selection

Big Endian Mode. Big endian mode is the native mode of the processor.

Little Endian Mode. The inverse assembler is designed to support both the native big endian mode and the little endian mode of operation. When operating in little-endian mode, the processor uses a technique known as "address munging" to convert internal little endian addresses into external big endian addresses. Internal and external addresses may differ from one another in the three least significant bits.

Little endian mode causes the instruction word from DL0...31 (DATA_B label; external address xxx4) to be dispatched before the instruction word from DH0...31 (DATA label; external address xxx0). It also causes byte and half-word reads and writes to appear on the opposite side of the bus and swaps the halves of double-word reads and writes. Setting the endian mode to **Little Endian** automatically compensates for these little endian operations.

AACK Mode Selection

Use this selection to tell the inverse assembler where to look for the AACK signal. This allows the inverse assembler to match the right address with the data for a transaction. In most systems, the AACK signal for a transfer comes before the data for that transfer. In this case, select the default mode **AACK before TA**. Some systems have a different implementation where the AACK comes after the corresponding data for a transaction. If your system uses this delayed AACK mode, select **AACK after TA**. In delayed AACK mode, the AACK for the current TA can be concurrent with the next TA, but the AACK cannot be delayed beyond the next TA.

Processor Revision Option

Use this section to tell the inverse assembler the revision of your target's MPC826X chip.

The EAV signal (available on MPC8260 rev. A.1 and higher) enables the full SDRAM address to appear on the bus in a single state. Enabling the EAV increases the inverse assembly speed, simplifies triggering, and enables the Source Viewer trigger setup to function correctly (see "Enabling full SDRAM

address" on page 34).

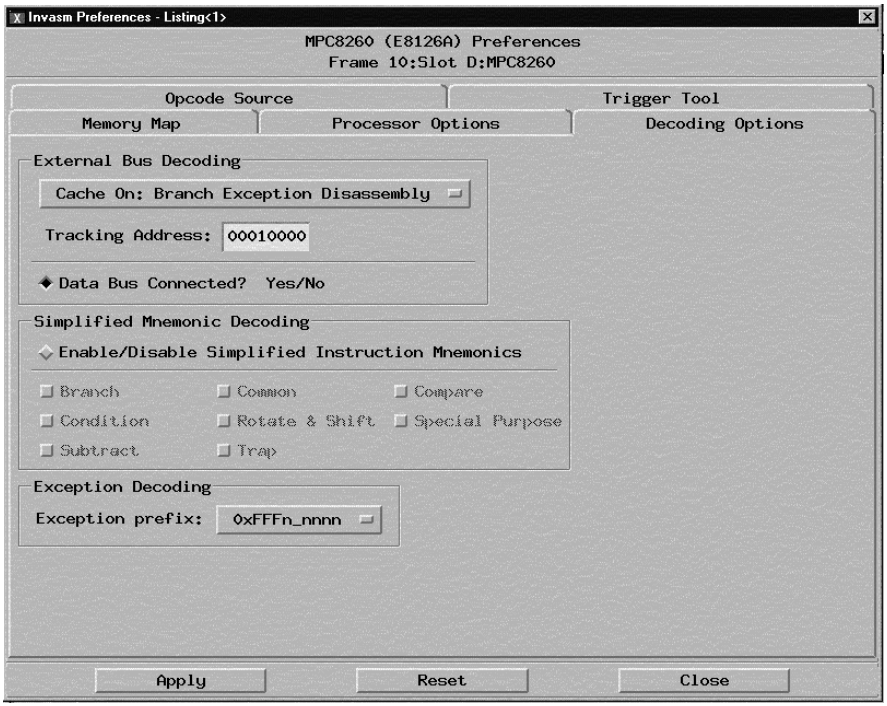
SDRAM Memory Parameters

If the target system has SDRAM memory and the full SDRAM address is not enabled (using rev. A.0 or EAV not enabled), use these selections to tell the inverse assembler the values of the SDAM and BSMA bits in the PSDMR register. The inverse assembler uses these values to reconstruct SDRAM addresses. This is required because SDRAM accesses break the address up into two separate cycles (see "Enabling full SDRAM address" on page 34).

Other Options

Use Analysis Probe Signals for pipeline tracking. As discussed earlier, the 60x Compatibility Mode can produce 2-level pipeline situations. In order for the inverse assembler to work when this situation occurs, the analysis probe must be connected and this option must be selected.

Decoding Options



External Bus Decoding. Choose **Cache Off: External Bus Disassembly** for traditional inverse assembly or **Cache On: Branch Exception Disassembly** for cache-on trace reconstruction, and provide the tracking address.

Data Bus Connected. Read and write states are always indicated regardless of whether the data bus is connected. However, when the data bus is connected, read/write data will also be displayed. See “Inverse Assembler Modes of Operation” on page 109.

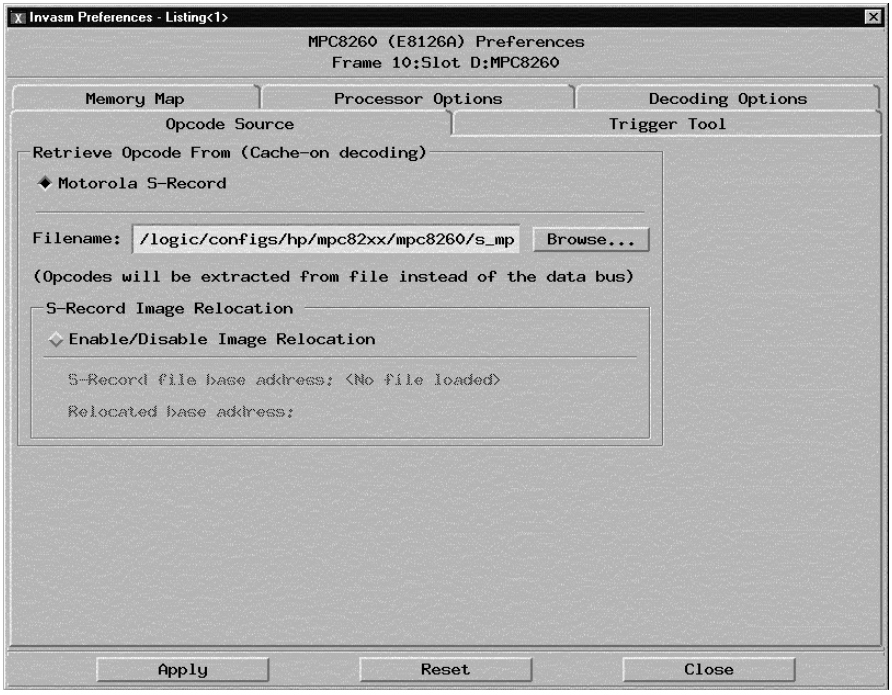
Simplified Mnemonic Decoding

Since the PowerPC instruction set has defined alternate mnemonics for some instructions, it may be helpful to display the simplified mnemonics to get a better idea of what a particular instruction is really doing. For example, an “or r1,r1,r1” instruction is simplified to a “nop.”

Exception Decoding

To provide better debugging with exceptions, the inverse assembler can output the types of exceptions that occur. Select the correct base of the exception table for this feature to be enabled.

Opcode Source



Specifying use of Motorola S-Record executable file. Select Motorola S-Record in the Retrieve Opcode From dialog to have a Motorola S-Record supply execution trace information to the cache-on trace reconstruction tool. Use the Browse... button to locate the S-Record file.

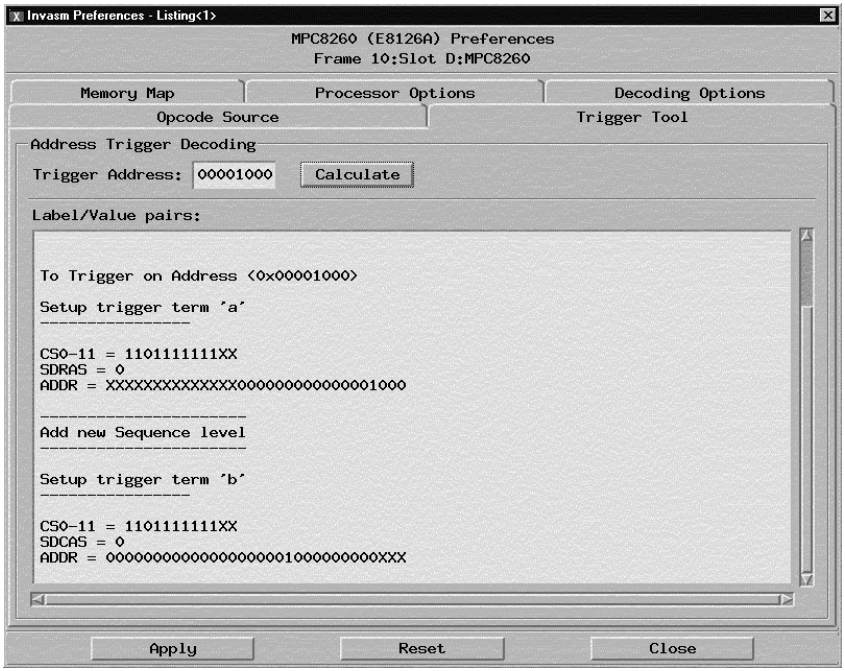
S-Record Image Relocation. The Image Relocation portion of the dialog box allows you to relocate the SREC file to some other location in memory. This is useful when the loaded file is moved to some other location in memory. For example, the starting address in the SREC file is 1000. However, memory starting at 1000 is relocated to 5000. In order for the inverse assembler to retrieve the correct data, the entire SREC file must be relocated to 5000. Enter the relocated base address; all the resulting offsets will be calculated by

the inverse assembler.

Trigger Tool

The Trigger Tool is an aide that helps you set up triggers more accurately for all types of memory. The Trigger Tool uses the addresses and memory types entered in the Memory Map window and determines additional qualifiers needed to better define the trigger address.

The Trigger Tool is especially useful when triggering on SDRAM addresses, where the address may be broken up into multiple cycles, requiring multiple trigger-sequence levels (see “Enabling full SDRAM address” on page 34). The Trigger Tool will guide you through setting up these more complicated triggers.



To enable/disable the instruction cache on the MPC826X

When the instruction cache is enabled, many PowerPC instructions are executed from the cache and do not appear on the external bus. To get an execution trace on the bus, the instruction cache can be disabled. This must be done in supervisor mode.

To disable the cache with a debugger:

Use your debugger to configure the HID0 register.

Register values for controlling the cache

Value	Meaning
0000 8000	Enable Instruction Cache
0000 4000	Enable Data Cache
0000 0800	Invalidate Instruction Cache
0000 0400	Invalidate Data Cache

To disable the cache with code:

- Disable the instruction cache with the following code:

```
mfspr    r3, hid0
rlwinm   r3, r3, 0, 17, 15  # clear bit 16 (ICE)
mtspr    hid0, r3
isync
```

- To also disable the data cache use:

```
mfspr    r3, hid0
rlwinm   r3, r3, 0, 18, 15  # clear ICE and DCE
mtspr    hid0, r3
isync
```

- To invalidate and disable both caches use:

```
mfspr   r3, hid0
ori     r3, 0C00# set ICFI and DCFI
mtspr   hid0, r3
rlwinm  r3, r3, 0, 22, 19  # clear ICFI and DCFI
mtspr   hid0, r3
rlwinm  r3, r3, 0, 18, 15   # clear ICE and DCE
mtspr   hid0, r3
isync
```

- Enable the instruction cache with the following code:

```
mfspr   r3, hid0
rlwinm  r3, r3, 1, 17, 15   # set ICE
mtspr   hid0, r3
isync
```

Loading Symbol Information

Symbols are more easily recognized than hexadecimal address values in logic analyzer trace displays, and they are easier to remember when setting up triggers.

Agilent Technologies logic analyzers let you assign user-defined symbol names to particular label values.

Also, you can download symbols from certain object file formats into logic analyzers.

To view predefined symbols for the MPC826X

User-defined symbols are symbols you create in the logic analyzer by assigning symbol names to label values. Typically, you assign symbol names to address label values, but you can define symbols for data, status, or other label values as well.

User-defined symbols are saved with logic analyzer configurations. The logic analyzer configuration files included with the MPC826X inverse assembler contain predefined symbols for logic analyzer labels.

To display the predefined symbols for the MPC826X:

1. Open the logic analyzer's **Setup** window.
2. Select the **Symbol** tab.
3. Select the **User Defined** tab.
4. Choose a label name from the Label list.

   The logic analyzer will display the symbols associated with the label.

Predefined Symbols Description		
Label	Encoding	Symbol
AACK	1	------
	0	Avalid
ARTRY	1	------
	0	Aretry
CAS0-7	0111 1111	CAS 0
	1011 1111	CAS 1
	1101 1111	CAS 2
	1110 1111	CAS 3
	1111 0111	CAS 4
	1111 1011	CAS 5
	1111 1101	CAS 6
	1111 1110	CAS 7
CS0-11	0111 1111 1111	CS 0
	1011 1111 1111	CS 1
	1101 1111 1111	CS 2
	1110 1111 1111	CS 3
	1111 0111 1111	CS 4
	1111 1011 1111	CS 5
	1111 1101 1111	CS 6
	1111 1110 1111	CS 7
	1111 1111 0111	CS 8
	1111 1111 1011	CS 9
	1111 1111 1101	CS 10
	1111 1111 1110	CS 11
DVAL	1	-----
	0	Dbeat
TA	1	------
	0	Dvalid
TBST	1	-----
	0	burst
TC1	0	data
	1	inst
TEA	1	-----
	0	error

Predefined Symbols Description		
Label	Encoding	Symbol
TSIZ03	0001	1 byte
	0010	2 byte
	0011	3 byte
	0100	4 byte
	0101	5 byte
	0110	6 byte
	0111	7 byte
	1001	16byte
	1010	24byte
	0000	8 byte

Predefined Symbols Description		
Label	Encoding	Symbol
TT	00000	cln blk
	00100	fsh blk
	01000	sync
	01100	kll blk
	10000	eieio
	10100	graf wr
	11000	TLB inv
	11100	graf rd
	00001	lwarx
	00101	reserv
	01001	tlbsync
	01101	icbi
	10001	reserv
	10101	reserv
	11001	reserv
	11101	reserv
	00010	wr flsh
	00110	wr kill
	01010	read
	01110	RWITM
	10010	wr flsh
	10110	reserv
	11010	rd atmc
	11110	RWITM a
	00011	reserv
	00111	reserv
	01011	RWNITC
	01111	reserv
	10011	reserv
	10111	reserv
	11011	reserv
	11111	reserv
TT RW	0	write
	1	read

To load object file symbols

The most common way to load program symbols into the logic analyzer is from an object file that is created when the program is compiled. The object file containing symbolic debug information must be in a format the logic analyzer understands.

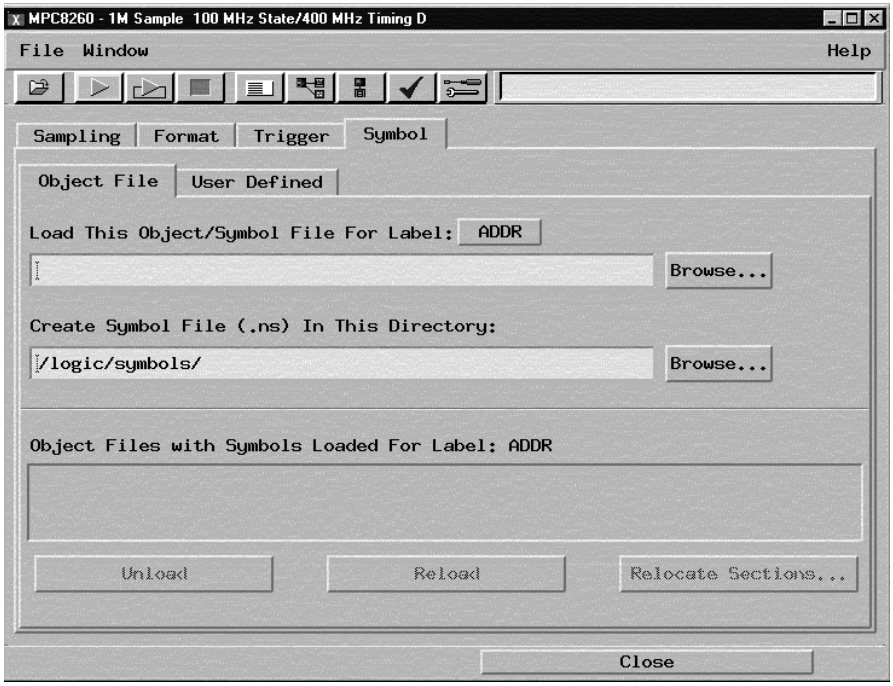
If your compiler generates object files in a format that the logic analyzer doesn't understand, you can use a General-Purpose ASCII (GPA) symbol file (see Chapter 8, "General-Purpose ASCII (GPA) Symbol File Format," on page 151).

To load symbols in the 16700-series logic analysis system:

1. Open the logic analyzer module's **Setup** window.
2. Select the **Symbol** tab.
3. Select the **Object File** tab.

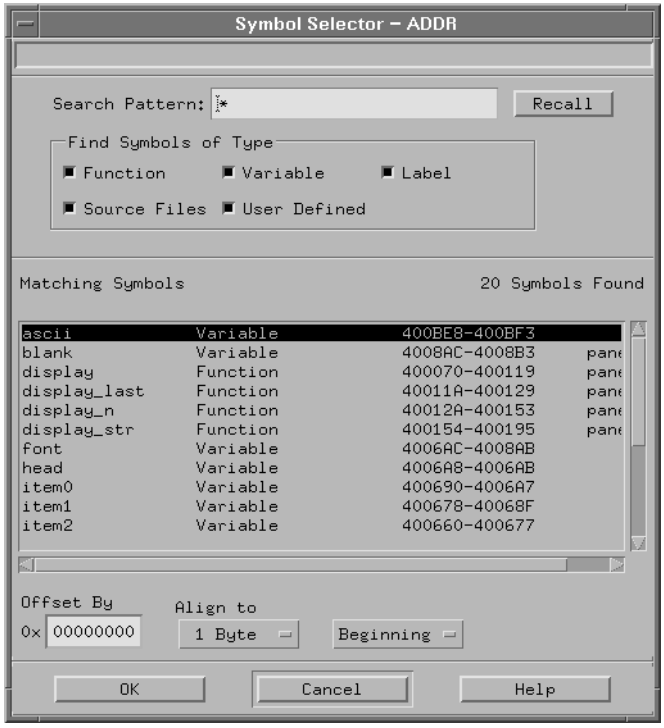
   Make sure the label is ADDR.

   From this dialog you can select object files and load their symbol information.



When you load object file symbols into a logic analyzer, a database of symbol/line number to address assignments is generated from the object file.

When defining trigger patterns, trigger ranges, and so on, the **Symbol Selector** dialog allows you to use a symbol in place of a hexadecimal value.



Changing the Analysis Mode

The logic analyzer can be set up to operate in the following analysis modes:

- State.
- Timing.

Inverse assembly is available in the state analysis mode.

To change to state analysis

In state mode, the logic analyzer uses the CLKIN signal from the MPC826X target system to capture data synchronously. This mode allows inverse assembly of MPC826X instructions and is the default mode set up by the configuration files.

To configure the logic analyzer for state mode:

1 Load the appropriate logic analyzer configuration file (see "To load configuration files (and the inverse assembler) from hard disk" on page 98).

The configuration files set up the rising edge of the J clock (J↑) as the master clock signal.

You can change the master clock setting in the logic analyzer's Setup window under the Sampling tab.

To change to timing analysis

In timing mode, the logic analyzer samples the microprocessor pins asynchronously, according to an internal, adjustable sample rate clock. The minimum sample period for a 250 MHz timing analyzer is 4 ns.

Inverse assembly is not available in the timing analysis mode.

The analysis mode is set in the Sampling tab of the logic analyzer Setup window.

To configure the logic analyzer for timing analysis:

1. Load the appropriate logic analyzer configuration file (see "To load configuration files (and the inverse assembler) from hard disk" on page 98).
2. Open the logic analyzer's **Setup** window.
3. Select the **Sampling** tab.
4. Change the selection from **State Mode** to **Timing Mode**.

6

Capturing MPC826X Execution

The normal steps in using the logic analyzer are:

1. Configure the logic analyzer.
2. Format labels for the logic analyzer channels (that is, mapping logic analyzer channels to target system signal names).
3. Load symbols from the program's object file.
4. Set up the trigger, and run the measurement.
5. Display the captured data.

With the MPC826X inverse assembler, the logic analyzer is configured, and labels are created (formatted) for the logic analysis channels when configuration files are loaded (see "To load configuration files (and the inverse assembler) from hard disk" on page 98).

You can load program object file symbols into the logic analyzer when configuring it (see "Loading Symbol Information" on page 122).

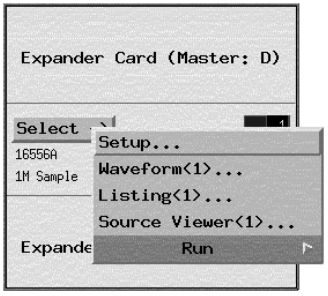
This chapter describes setting up logic analyzer triggers when using the inverse assembler and the B4620B source correlation tool set.

See Chapter 7, "Displaying Captured MPC826X Execution," on page 141 for information on displaying captured data.

Setting Up Logic Analyzer Triggers

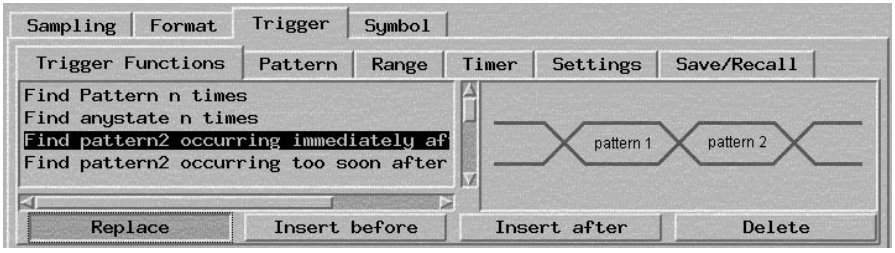
To set up logic analyzer triggers

1 Open the logic analyzer's Setup window.

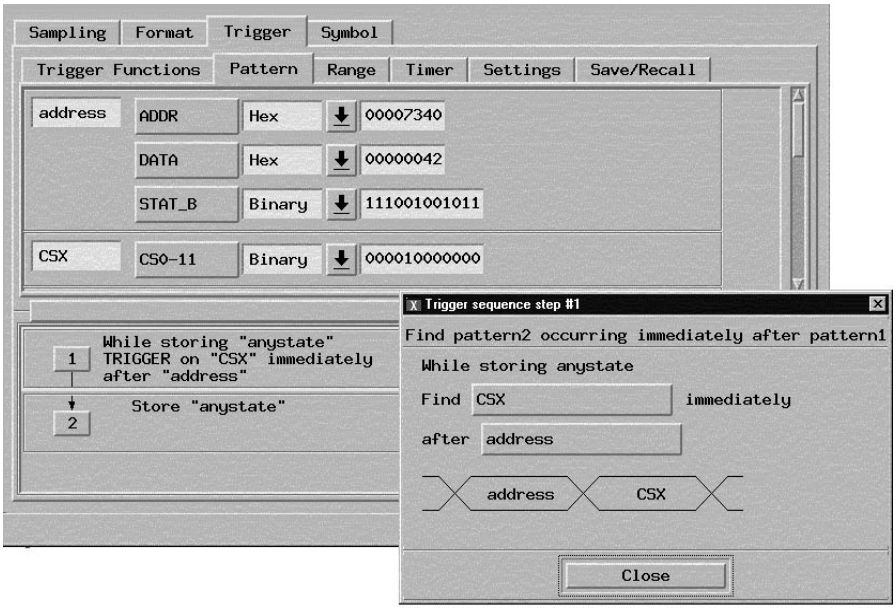


2 Select the Trigger tab.

3 Select the trigger function that will be used in the logic analysis measurement.



4 Set up the trigger sequence.



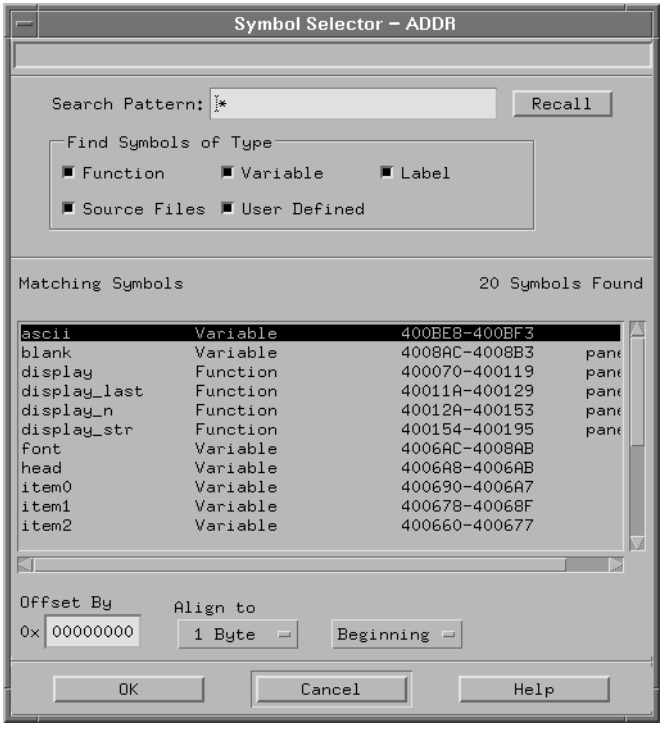
5 Run the measurement.

See Also

The 16700-series logic analysis system's on-line help for more information on setting up logic analyzer triggers.

To compensate for relocated code

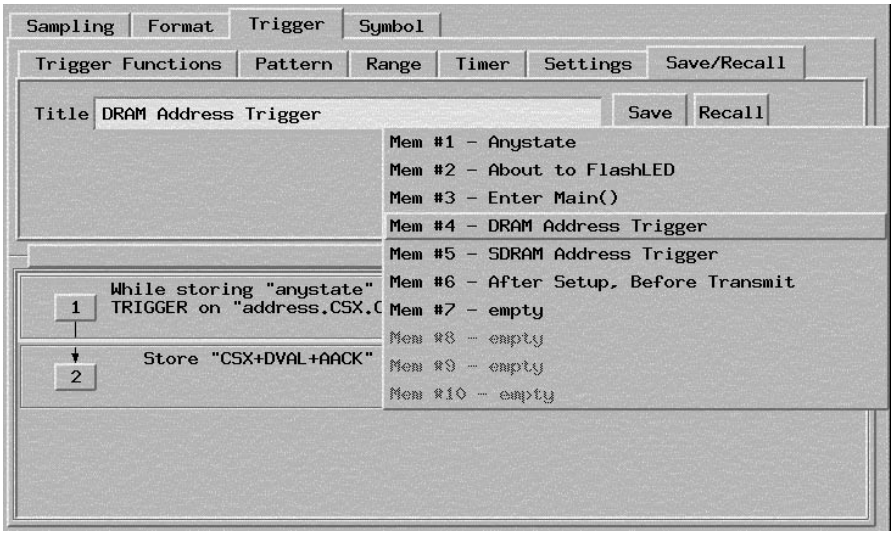
When code segments are relocated, or when memory management units produce fixed code offsets, you can compensate by using the address offset field in the Symbol Selector dialog.



Entering the appropriate address offset will cause the logic analyzer to reference the correct symbol information for the relocatable or offset code.

Using the Saved Trigger Specifications

Logic analyzer configuration files for the MPC826X contain saved trigger specifications. You can recall these trigger specifications using the Save/Recall tab under the Trigger tab.



Anystate

This is the default trigger specification. Any captured state will trigger the logic analyzer and any state after that is stored. It gives you an easy way to return to the default.

Data Trigger

This trigger specification will trigger on a DVAL value of zero and the chip select and data values you specify as pattern values. States that match the specified chip select value, DVAL=0, or AACK=0 are stored.

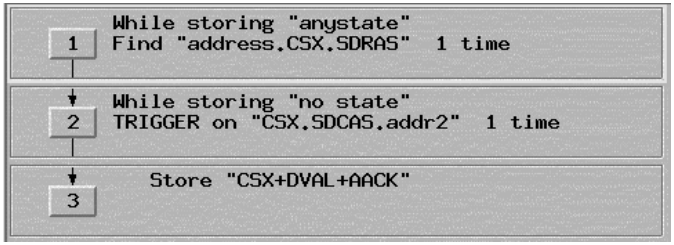
Flash/ROM Address Trigger/60x Mode Addr Trig

This trigger specification will trigger on AACK=0 and the address and chip select values you specify as pattern values. States that match the specified chip select value, DVAL=0, or AACK=0 are stored.

DRAM Address Trigger

This trigger specification will trigger on the address, chip select, and column address strobe values you specify as pattern values. States that match the specified chip select value, DVAL=0, or AACK=0 are stored.

SDRAM Address Trigger



This trigger specification is used when triggering on SDRAM addresses.

The trigger is designed to be used when the full SDRAM address is *not* valid on a single cycle (using revision A.0 or EAV not enabled — see “Enabling full SDRAM address” on page 34). In this case, triggering on SDRAM addresses is more complicated because the address is broken up into 2 cycles. This trigger specification adds a level to the trigger sequence.

This trigger can be modified to be used when the full SDRAM address *is* valid on a single cycle (see “Enabling full SDRAM address” on page 34). In this case, simply remove the first sequence trigger level.

The first sequence level looks for SDRAS=0 and the address and chip select values you specify. After a captured state matches the first level, the second sequence level looks for SDCAS=0 and the chip select and second address values you specify. After a captured state matches the second level, the logic analyzer triggers, and states that match the specified chip select value, DVAL=0, or AACK=0 are stored.

The inverse assembler Preferences dialog has a Trigger Tool tab that will show you the correct trigger values to use on a particular SDRAM address (see

"Trigger Tool" on page 119).

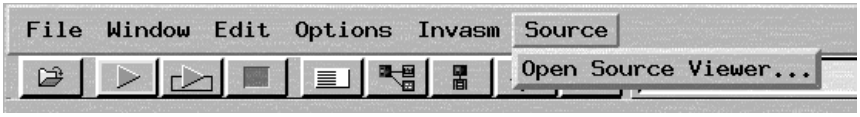
Triggering on Source Code

When setting up trigger specifications to capture MPC826X execution:

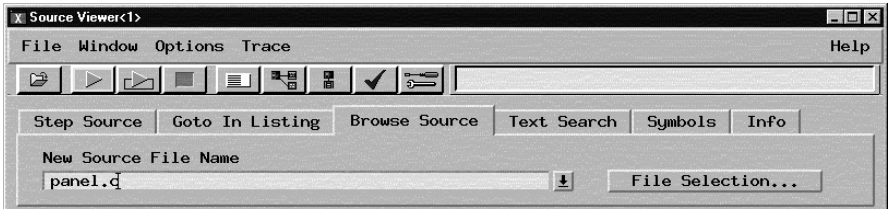
- Use the logic analyzer storage qualification to capture the software execution you're interested in and filter out library code execution (whose source file lookups can take a long time if the library source code is not available).

To set up triggers based on source code

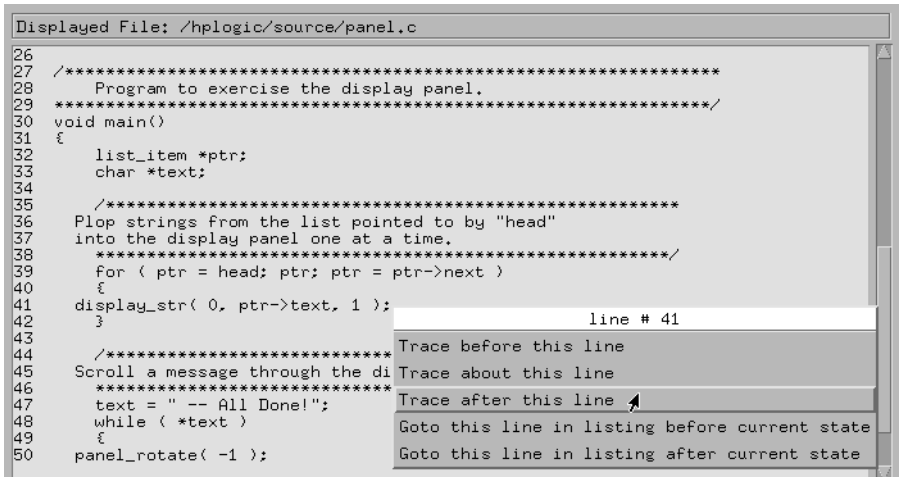
1 Open the Source Viewer window.



2 Browse the source file that contains the code you want to trigger on.



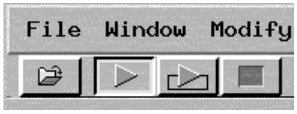
3 Click the source code line you want to trigger on and specify whether you want to trace before, about or after the line. Or, use the Source Viewer's Trace menu to trace about a variable, function, or line number.



NOTE: Source Viewer trigger setup commands will only work for code in SDRAM if the full SDRAM address has been enabled. See "Enabling full SDRAM address" on page 34.

If the full SDRAM address is not enabled, source viewer trigger setup commands will not work for code in SDRAM because the address is broken up into two cycles. See "SDRAM Address Trigger" on page 137.

4 Run the measurement.



To avoid capturing library code execution

When viewing the source code associated with captured data, the source correlation tool set can exhibit long response times to requests for the next source line if the current trace listing corresponds to code from a library that is not in the source code search path. Logic analyzer storage qualification can be used to avoid capturing library code routines.

You should also configure the logic analyzer's storage qualification capabilities

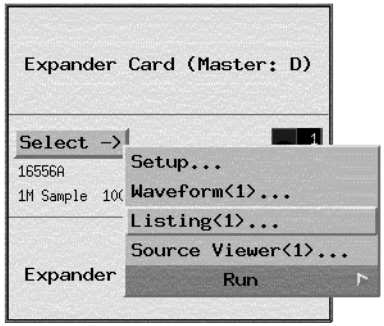
to store only those cycles that correspond to software execution (non-idle, etc.).

7

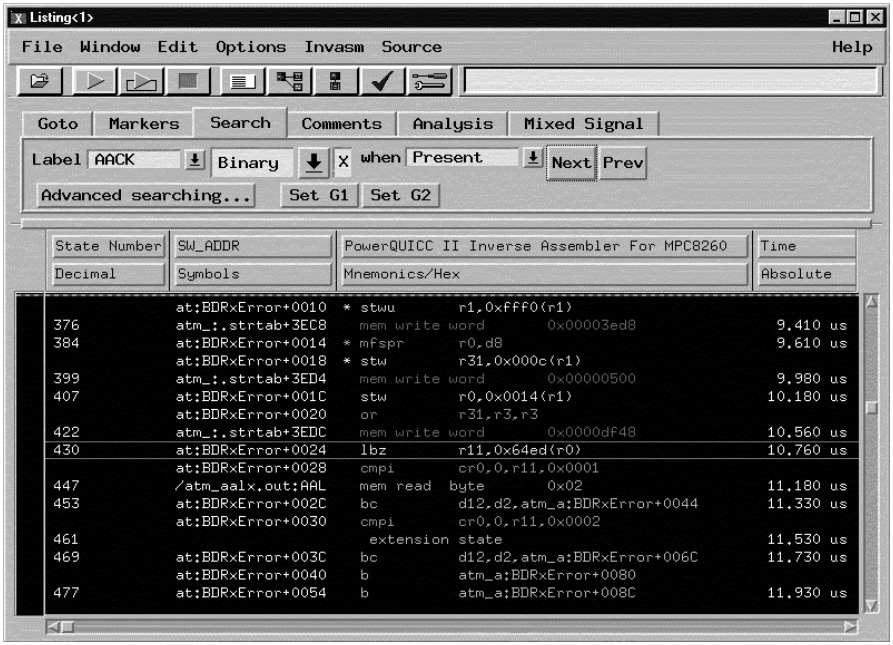
Displaying Captured MPC826X Execution

To display the captured state data

1 Open the Listing display window.



The logic analyzer displays captured state data in the Listing display.



The inverse assembler is already loaded when state configuration files are loaded, but it can also be loaded into a Listing display using the Invasm menu.

The name of the inverse assembler file is I8620E, and it is located in the /logic/ia directory.

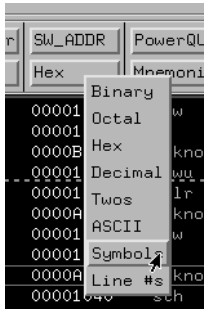
See Also

"To use the inverse assembler filters" on page 144 for information on displaying or hiding certain types of microprocessor bus cycles.

The 16700-series logic analysis system on-line help for information on using the Listing display.

To display symbols

- Over a Listing display's label base, right-click the mouse button, and select Symbols.



Any symbols that have been defined will be displayed for equivalent captured values.

See Also

"To load object file symbols" on page 126.

To interpret the inverse assembled data

General purpose registers are displayed as r0, r1, ..., r31. Floating point registers are displayed as f0, f1, ..., f31. Condition registers are displayed as cr0, cr1, ..., cr7. Special purpose registers are displayed using their mnemonic.

Most numerical data is displayed in hexadecimal, for example, "lwz r28, 0x0044(r1)."

Bit numbers and shift counts are displayed in decimal with a “d” prefix, for example, “cror d31,d31,d31.”

A few instructions display their operands in binary with a “b” prefix, for example, “mtfsfi 4,b0101.”

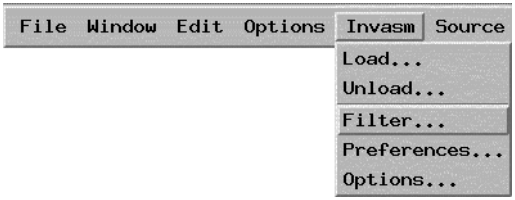
The inverse assembler decodes the full 32-bit mode PowerPC instruction set architecture. Instructions that are 64-bit mode or optional instructions not implemented on the MPC826X are decoded as “illegal”. Any instruction that does not decode to a valid opcode is shown as “unknown”.

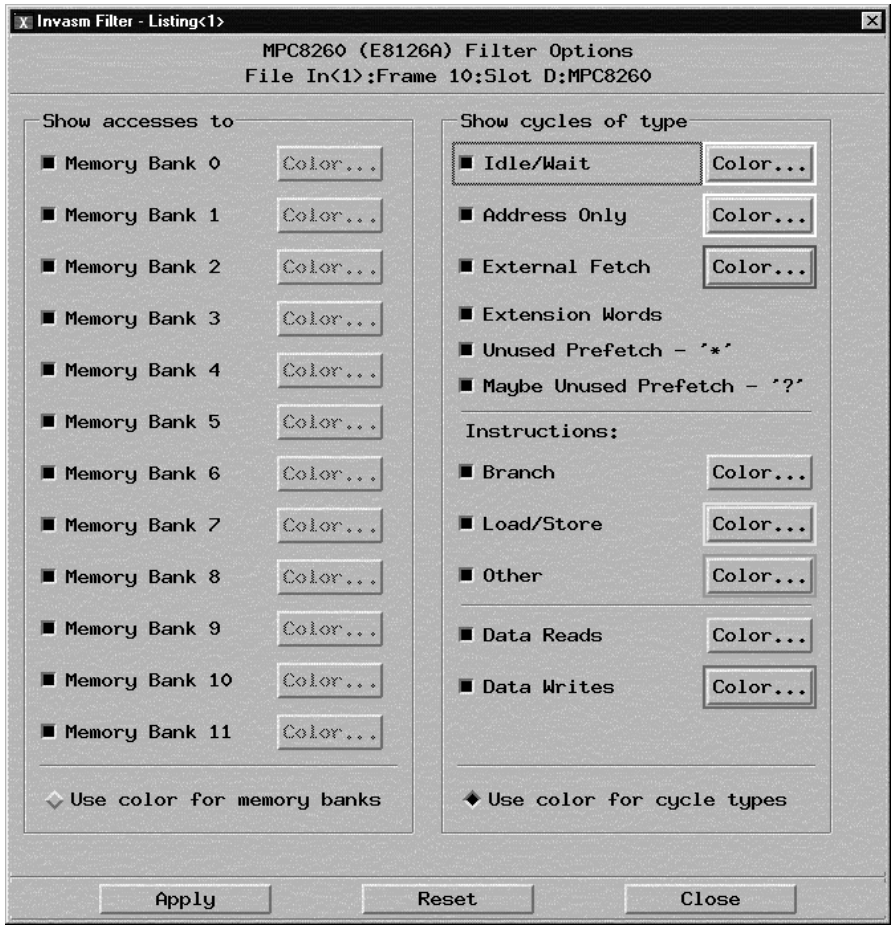
When these unimplemented opcodes are encountered, the instruction mnemonic has a “?” prefix. If a reserved bit is set in an instruction opcode field, a “?” is appended most often to the mnemonic, but in some cases to an operand.

An instruction word of 00000000 is decoded as “illegal.” Otherwise, if an opcode is invalid, it is shown as “Undefined Opcode.”

To use the inverse assembler filters

- In the Listing display window, choose the Filter command from the Invasm menu.





The inverse assembler filtering options allow you to display or hide certain types of microprocessor bus cycles or memory bank accesses.

Because the filter options do not affect the data that is stored by the logic analyzer (they only affect whether that data is displayed), they let you display the same data in different ways.

Filtering allows faster analysis in two ways:

- Unneeded information can be taken out of the display. For example, suppressing idle/wait states will let you view more instruction cycles in each screenful.
- Particular operations can be isolated by suppressing all other operations. For example, Branch instructions can be shown, with all other states suppressed, allowing quick analysis of branch instructions.

You can also use color to distinguish between cycle types or memory bank accesses (when they are displayed). Color can be used for distinguishing between memory bank accesses or cycle types, but not both at the same time.

You can display or hide the following types of cycles:

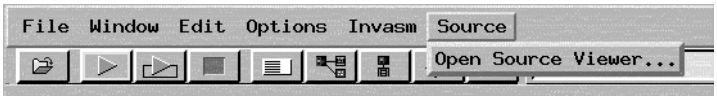
- Idle/Wait States.
- Address Only States.
- External Fetch (cache line fills).
- Extension Words.
- Branch Instructions.
- Load/Store Instructions.
- Other Instructions.
- Data Reads.
- Data Writes.

See Also

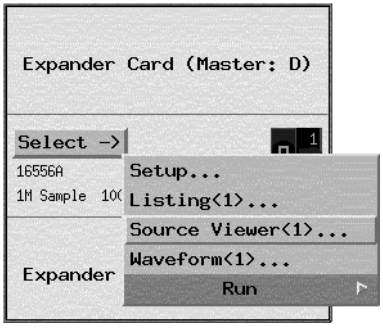
The address ranges for memory banks 0-11 are specified in the Preferences menu (see “Setting Inverse Assembler Preferences” on page 111).

To view the source code associated with captured data

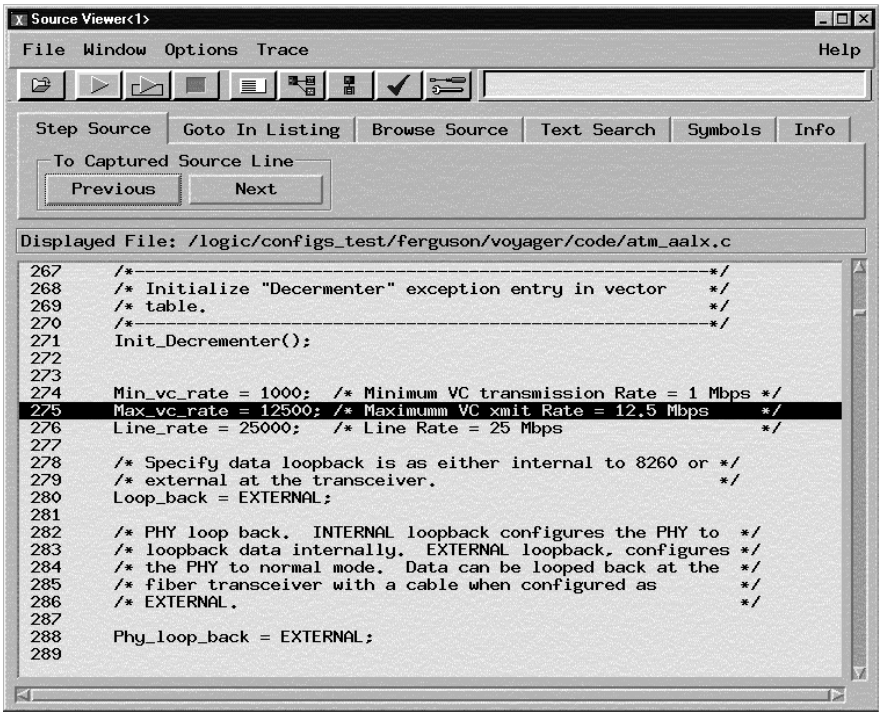
- In the Listing display window, select Source Viewer from the Source menu.



- Or, open the Source Viewer window from the logic analyzer's icon in the main system window.



The source correlation tool set correlates the logic analyzer's address label with a line of high-level source code whose address, symbol name, file name, and line numbers are described in a symbol file downloaded to the logic analyzer (see "To load object file symbols" on page 126).



Inverse Assembler Generated SW_ADDR (Software Address) Label

In the 6600A/16700-series logic analysis system, the MPC826X inverse assembler generates a “SW_ADDR” label. The SW_ADDR label is displayed as another column in the Listing tool. This label is also known as the software address generated by the inverse assembler.

The “Goto this line in listing” commands in the 16700-series logic analysis system perform a pattern search on the SW_ADDR label in the Listing display (when an inverse assembler is loaded). Because the inverse assembler is called for each line that is searched, the search can be slow, especially with a deep memory logic analyzer.

Also, a single line of source code will generate many assembly instructions. The “Goto this line in listing” commands will not find a given line of source code unless the first assembly instruction generated from the source line has been acquired by the logic analyzer.

For example, if the compiler unrolls a loop in the source code, the trace could

begin after the first assembly instruction of the loop has been executed. A "Goto this line in listing" command would not find the source line.

Access to Source Code Files

The source correlation tool set must be able to access the high-level source code files referenced by the symbol information so that these source files can be displayed next to and correlated with the logic analyzer's execution trace acquisition. This requires you to be aware of a number of issues.

Source File Search Path. Verify that the correct file search paths for the source code have been entered into the source correlation tool set. The B4620B source correlation tool set can often read and access the correct source code file from information contained in the symbol file if the source code files have not been moved since they were compiled.

Network Access to Source Files. If source code files are being referenced across a network, the logic analyzer networking must be compatible with the user's network environment. Agilent Technologies logic analyzers currently support Ethernet networks running a TCP/IP protocol and support ftp, telnet, NFS client/server and X-Window client/server applications. Some PC networks may require extensions to the normal LAN protocols to support the TCP/IP protocol and/or these networking applications. Users should contact their LAN system administrators to help set up the logic analyzer on their network.

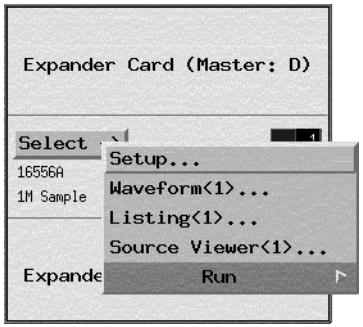
Source File Version Control. If the source code files are under a source code or version control utility, check the file names and paths carefully. These utilities can change source code file paths and file names. If these names are changed from the information contained in the symbol file, the source correlation tool set will not be able to find the proper source code file. These version control utilities usually provide an "export" command that creates a set of source code files with unmodified names. The source correlation tool set can then be given the correct path to these files.

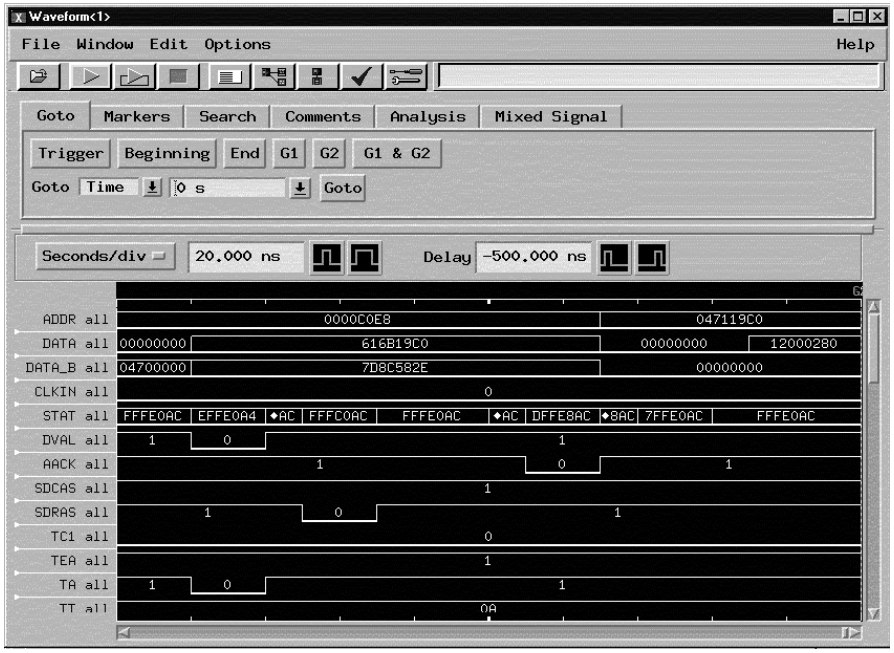
See Also

More information on configuring and using the source correlation tool set can be found in the on-line help for your logic analysis system.

To display captured timing analysis mode data

- Open the Waveform display for your logic analyzer.





You can also use the Waveform display in the state analysis mode to display state timing diagrams

8

General-Purpose ASCII (GPA) Symbol File Format

General-purpose ASCII (GPA) format files are loaded into a logic analyzer just like other object files, but they are usually created differently.

If your compiler does not include symbol information in the output, or if you want to define a symbol not in the object file, you can create an ASCII format symbol file.

Typically, ASCII format symbol files are created using text processing tools that convert compiler or linker map file output that has symbolic information.

You can typically use symbol table information from a linker map file to create a General-Purpose ASCII (GPA) symbol file.

Various kinds of symbols are defined in different records in the GPA file. Record headers are enclosed in square brackets; for example, [VARIABLES]. For a summary of GPA file records and associated symbol definition syntax, refer to the "GPA Record Format Summary" that follows.

Each entry in the symbol file must consist of a symbol name followed by an address or address range.

While symbol names can be very long, the logic analyzer only uses the first 16 characters.

The address or address range corresponding to a given symbol appears as a hexadecimal number. The address or address range must immediately follow the symbol name, appear on the same line, and be separated from the symbol name by one or more blank spaces or tabs. Ensure that address ranges are in the following format:

```
beginning address..ending address
```

Example

```
main 00001000..00001009
test 00001010..0000101F
var1 00001E22 #this is a variable
```

This example defines two symbols that correspond to address ranges and one point symbol that corresponds to a single address.

For more detailed descriptions of GPA file records and associated symbol definition syntax, refer to these topics that follow:

- SECTIONS
- FUNCTIONS
- VARIABLES
- SOURCE LINES
- START ADDRESS
- Comments

GPA Record Format Summary

Format

```
[SECTIONS]
section_name start..end attribute

[FUNCTIONS]
func_name start..end

[VARIABLES]
var_name start [size]
var_name start..end

[SOURCE LINES]
File: file_name
line# address

[START ADDRESS]
address

#Comments
```

If no record header is specified, [VARIABLES] is assumed. Lines without a preceding header are assumed to be symbol definitions in one of the VARIABLES formats.

Example

This is an example GPA file that contains several different kinds of records:

```
[SECTIONS]
prog     00001000..0000101F
data     40002000..40009FFF
common   FFFF0000..FFFF1000

[FUNCTIONS]
main     00001000..00001009
test     00001010..0000101F

[VARIABLES]
total    40002000 4
value    40008000 4

[SOURCE LINES]
File: main.c
10       00001000
11       00001002
14       0000100A
22       0000101E

File: test.c
5        00001010
7        00001012
11       0000101A
```

SECTIONS

Format

```
[SECTIONS]
section_name start..end attribute
```

Use SECTIONS to define symbols for regions of memory, such as sections, segments, or classes.

`section_name` A symbol representing the name of the section.

`start` The first address of the section, in hexadecimal.

`end` The last address of the section, in hexadecimal.

`attribute` This is optional, and may be one of the following:

NORMAL (default)—The section is a normal, relocatable section, such as code or data.

NONRELOC—The section contains variables or code that cannot be relocated; this is an absolute segment.

Enable Section Relocation
To enable section relocation, section definitions must appear before any other definitions in the file.

Example

```
[SECTIONS]
prog          00001000..00001FFF
data          00002000..00003FFF
display_io    00008000..0000801F NONRELOC
```

If you use section definitions in a GPA symbol file, any subsequent function or variable definitions must be within the address ranges of one of the defined sections. Functions and variables that are not within the range are ignored.

FUNCTIONS

Format

```
[FUNCTIONS]
func_name   start..end
```

Use FUNCTIONS to define symbols for program functions, procedures, or

subroutines.

`func_name` A symbol representing the function name.

`start` The first address of the function, in hexadecimal.

`end` The last address of the function, in hexadecimal.

Example

```
[FUNCTIONS]
main     00001000..00001009
test     00001010..0000101F
```

VARIABLES

Format

```
[VARIABLES]
var_name   start [size]
var_name   start..end
```

You can specify symbols for variables either by using the address of the variable, the address and the size of the variable, or a range of addresses occupied by the variable. If you specify only the address of a variable, the size is assumed to be one byte.

`var_name` A symbol representing the variable name.

`start` The first address of the variable, in hexadecimal.

`end` The last address of the variable, in hexadecimal.

`size` This is optional, and indicates the size of the variable, in bytes, in decimal.

Example

```
[VARIABLES]
subtotal     40002000 4
total        40002004 4
data_array   40003000..4000302F
status_char  40002345
```

SOURCE LINES

Format

```
[SOURCE LINES]
File: file_name
line# address
```

Use SOURCE LINES to associate addresses with lines in your source files.

`file_name` The name of a file.

`line#` The number of a line in the file, in decimal.

`address` The address of the source line, in hexadecimal.

Example

```
[SOURCE LINES]
File: main.c
10       00001000
11       00001002
14       0000100A
22       0000101E
```

START ADDRESS

Format

```
[START ADDRESS]
address
```

`address` The address of the program entry point, in hexadecimal.

Example

```
[START ADDRESS]
00001000
```

Comments

Format

```
#comment text
```

Use the # character to include comments in a file. Any text following the # character is ignored. You can put comments on a line alone or on the same line following a symbol entry.

Example

```
#This is a comment.
```

9

Troubleshooting the Logic Analyzer

If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

If you still have difficulty using the analyzer after trying the suggestions in this chapter, please contact your local Agilent Technologies service center.

CAUTION: When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, and probes. Otherwise, you may damage circuitry in the logic analyzer or target system.

Solving Logic Analyzer Problems

This section lists general logic analyzer problems that you might encounter.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ❏ Remove and reseat all cables and probes, ensuring that there are no bent pins or poor connections.
- ❏ Adjust the threshold level of the data pod to match the logic levels in the system under test.
- ❏ Use an oscilloscope to check the signal integrity of the data lines.

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also

See “Capacitive loading” on page 166 for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

- ❏ Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.

  The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

No activity on activity indicators

- ❏ Check for loose cables or board connections.
- ❏ Check for bent or damaged pins.

No trace list display

If there is no trace list display, it may be that your trigger specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ❏ Check your trigger sequencer specification to ensure that it will capture the events of interest.
- ❏ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Analyzer won't power up

If logic analyzer power is cycled when the logic analyzer is connected to a target system or emulation probe that remains powered up, the logic analyzer may not be able to power up. Some logic analyzers are inhibited from powering up when they are connected to a target system or emulation probe that is already powered up.

- ❏ Remove power from the target system; then, disconnect all logic analyzer cabling from the target system. This will allow the logic analyzer to power up. Reconnect logic analyzer cabling after power up.

Solving Probing Problems

This section lists probing problems that you might encounter when using a logic analyzer. If the solutions suggested here do not correct the problem, you may have a damaged logic analyzer. Contact your local Agilent Technologies Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the target system, the microprocessor (if socketed) or the probe cables may not be installed properly, or they may not be making electrical contact.

❏ Ensure that you are following the correct power-on sequence for the logic analyzer and target system.

1. Power up the logic analyzer.
2. Power up the target system.

If you power up the target system before you power up the logic analyzer, interface circuitry may latch up and prevent proper target system operation.

❏ Verify that the logic analyzer cables are in the proper target system connector headers and are firmly inserted.

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

- ❏ Do a full reset of the target system before beginning the measurement.

  Some designs require a full reset to ensure correct configuration.

- ❏ Ensure that your target system meets the timing requirements of the processor with the logic analyzer connected.

  See "Capacitive loading" on page 166. While logic analyzer probe loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

- ❏ Ensure that you have sufficient cooling for the microprocessor.

  Ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the logic analyzer, or system lockup in the microprocessor. All logic analyzer probes add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- ❏ Remove as many pin protectors, extenders, and adapters as possible.

Solving Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the logic analyzer or in your target system. If you follow the suggestions in this section to ensure that you are using the logic analyzer and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem may be due to incorrect synchronization, modified configuration, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

- ❏ Ensure that each logic analyzer pod is connected to the correct connector.

  There is not always a one-to-one correspondence between analyzer pod numbers and probe cable numbers. Probes must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order. The cable connections for each probe are often altered to support that need. Thus, one probe might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See "Connecting the Logic Analyzer to the Target System" on page 71 for connection information.

- ❏ Check the activity indicators for status lines locked in a high or low state.

- ❏ Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels.

Some inverse assemblers also require other data labels. See Chapter 5, "Configuring the Logic Analyzer," on page 95 for more information.

❑ Verify that all microprocessor caches and memory managers have been disabled.

In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly; however, it may be incorrect because a portion of the execution trace was not visible to the logic analyzer.

❑ Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

❑ Ensure that the inverse assembler is on the same disk as the configuration files you are loading.

Configuration files for the state analyzer contain a pointer to the name of the corresponding inverse assembler. If you delete the inverse assembler or rename it, the configuration process will fail to load the disassembler.

See Chapter 5, "Configuring the Logic Analyzer," on page 95 for details.

Solving Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

❏ Adjust the skew in the Intermodule menu.

You may be able to specify a skew value that enables the event to be captured.

❏ Change the trigger specification for modules upstream of the one with the problem.

If you are using a logic analyzer to trigger the oscilloscope, try specifying a trigger state one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and not always be related to the event you are trying to capture with the oscilloscope.

Logic Analyzer Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file.

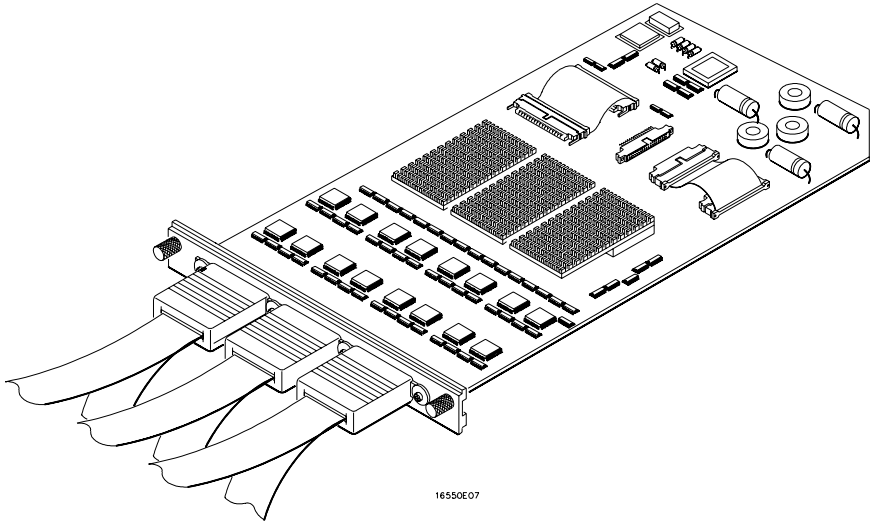
Ensure that the inverse assembler file is not renamed or deleted, and that it is located in the correct directory:

- For 16700-series logic analysis systems it should be in /logic/ia.
- For other logic analyzers it should be in the same directory as the configuration file.

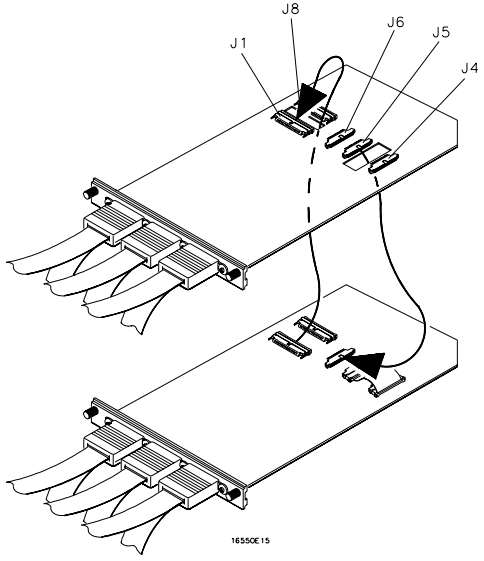
"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly for one or two 16550A logic analyzer cards. The following diagrams show the correct cable connections for one-card and two-card installations. Ensure that your cable connections match the silk-screened labels on the card, and that they are fully seated in the connectors. Then, repeat the measurement.

Cable Connections for One-Card 16550A Installations



Cable Connections for Two-Card 16550A Installations



See Also

The *16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide*.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ❏ Verify that the appropriate module has been selected from the Load {module} from File {filename} in the disk operation menu. Selecting Load {All} will cause incorrect operation when loading most configuration files.

See Also

See Chapter 5, "Configuring the Logic Analyzer," on page 95 for a description of how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

- ❏ This error message might occur if the logic analyzer cards are not firmly seated in the 16700-series logic analysis system frame or in the 16701A expansion frame. Ensure that the cards are firmly seated.
- ❏ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- ❏ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the target system. See "Connecting the Logic Analyzer to the Target System" on

page 71 to determine the proper connections.

"Time from Arm Greater Than 41.93 ms"

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- ❏ When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.

See Also

See Chapter 10, "Service Guide," beginning on page 175 for information on getting help from Agilent Technologies.

10

Service Guide

To return a part to Agilent Technologies for service

1. Follow the procedures in the "Solving Problems" chapter to make sure that the problem is caused by a hardware failure and not by configuration or cabling problems.
2. Get the address of the nearest Agilent Technologies service center. To locate a sales or service office near you, go to the world-wide web site:

   http://www.tm.agilent.com

   and select Contact Us.
3. Package the part and send it to the Agilent Technologies service center.

   Keep any parts which you know are working.
4. When the part has been replaced, it will be sent back to you. The replacement part will have the same serial number as the part you sent for repair.

   In some parts of the world, on-site repair service is available. Ask an Agilent Technologies sales or service representative for details.

To get replacement parts

The following table lists some parts that may be replaced if they are damaged or lost. The part numbers are subject to change. Contact your nearest Agilent Technologies sales office for further information. To locate a sales or service office near you, go to the world-wide web site:

http://www.tm.agilent.com

and select Contact Us.

Analysis Probe Replacement Parts

HP Part Number	Description
E5346A	High-density cable
E8125-69503	Analysis probe circuit board (exchange)
E8125-87606	480-pin TBGA double header
E8125-87607	480-pin TBGA extender
E8125-87613	BGA carrier (also called LS pack connection adapter)
E8160-60001	BGA probing kit

NOTE: See the figure on page 20 for an illustration of most of these replacement parts.

Contacting Agilent Technologies

If the analysis probe still does not work after following the troubleshooting steps in this chapter:

1. Note that the inverse assembler product number is E8126A and the analysis probe model number is E8125A. Write down your target processor type and version.
2. Call your nearest Agilent Technologies sales or service office.

   To locate a sales or service office near you, go to the world-wide web site:

   http://www.tm.agilent.com

   and select Contact Us.

11

Specifications and Characteristics

Operating Characteristics

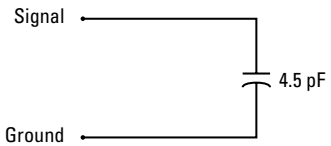
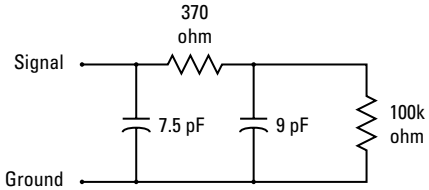
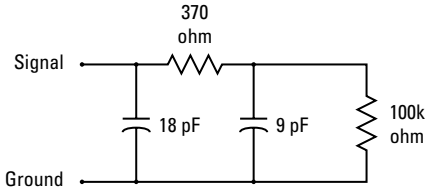
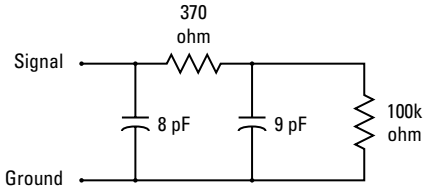
The following operating characteristics are not specifications, but are typical operating characteristics for the E8125A analysis probe for the MPC826X PowerQUICC II.

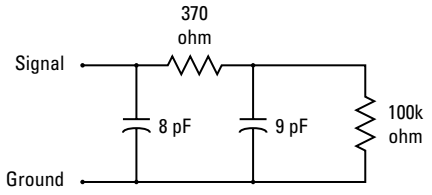
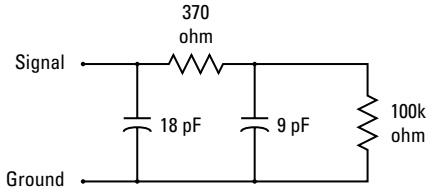
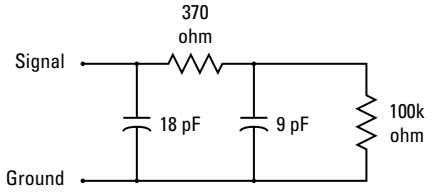
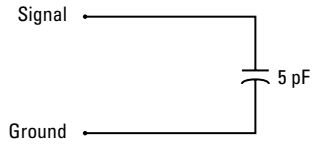
Operating Characteristics	
Microprocessor Compatibility	Motorola PowerQUICC II Processors listed on page 3.
Package Supported	480-pin BGA
Microprocessor Bus Speed	66 MHz maximum
Logic Analyzers Supported	16550A (2 cards) 16554A/55A/55D (2 or 3 cards) 16556AD/56D/57D (2, 3, or 4 cards) 16600A 16601A 16710A/11A/12A (2 cards) 16715A/16A/17/18/19A (2, 3, 4, or 5 cards) 16750/51/52 (2, 3, 4, or 5 cards)
Accessories Required	For state and timing analysis, the E8160A BGA probing kit and the E5346A high-density cables are required (included with the E8125A).
Optional Accessories	The E3453B emulation probe can be connected to the analysis probe.
Probes Required	Eight 16-channel probes are required for disassembly of MPC8260 PowerQUICC II. Fourteen additional 16-channel pods are available.

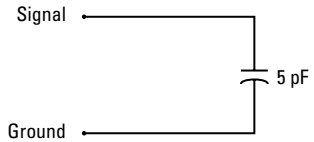
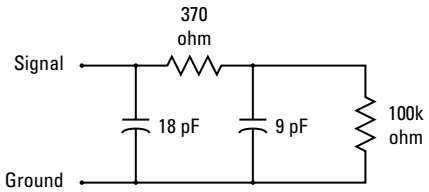
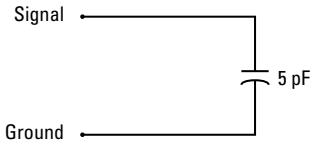
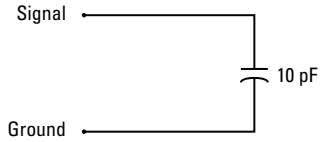
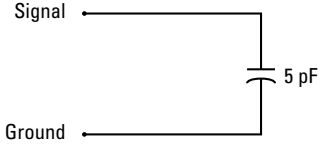
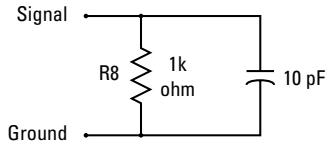
Electrical Characteristics	
Power Requirements	500 mA @ 5V, supplied by the logic analyzer. CAT I: mains isolated.
Signal Line Loading	(See the processor signal line loading table that follows.)

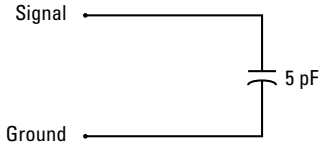
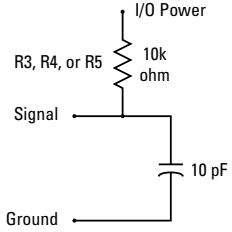
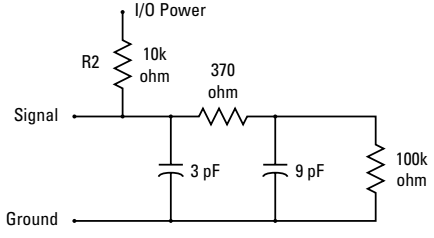
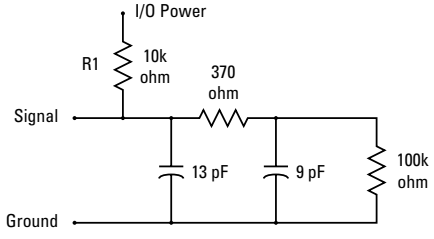
Environmental Characteristics	
Temperature, Operating	0 to + 50 degrees C +32 to +122 degrees F
Altitude, Operating	4,600 m 15,000 feet
Humidity	Up to 75% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board.
Pollution	IEC Pollution degree 2. Normally only dry non-conductive pollution occurs. Occasionally a temporary conductivity caused by condensation may occur. Indoor use only.

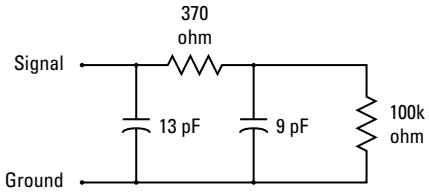
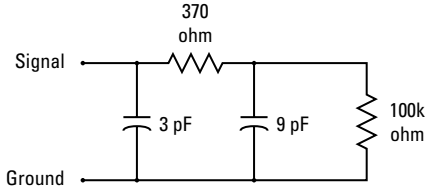
Processor Signal Line Loading

Signal	MPC8260 Pin	Analysis Probe DIP Switch	Equivalent Load (includes logic analyzer)
CLKIN	AH4	N/A	
LCL_ADDR [27]/PCI_CLK	AA25	N/A	
CKSTOP_OUT (pin D21)	D21	S5 = OFF	
		S5 = ON	

Signal	MPC8260 Pin	Analysis Probe DIP Switch	Equivalent Load (includes logic analyzer)
CKSTOP_OUT (pin R26)	R26	S5 = OFF	
		S5 = ON	
ADDR[27] ADDR[28] ADDR[29] ADDR[30] ADDR[31]	P1 R1 R3 R5 R4	S3 = OFF	
		S3 = ON	

Signal	MPC8260 Pin	Analysis Probe DIP Switch	Equivalent Load (includes logic analyzer)
BADDR[27] BADDR[28] BADDR[29] BADDR[30] BADDR[31]	T5 U1 U2 U3 U4	S3 = OFF	
		S3 = ON	
TDO*	AF5	S1 = OFF	
		S1 = ON	
TDI*	AE6	S1 = OFF	
		S1 = ON	

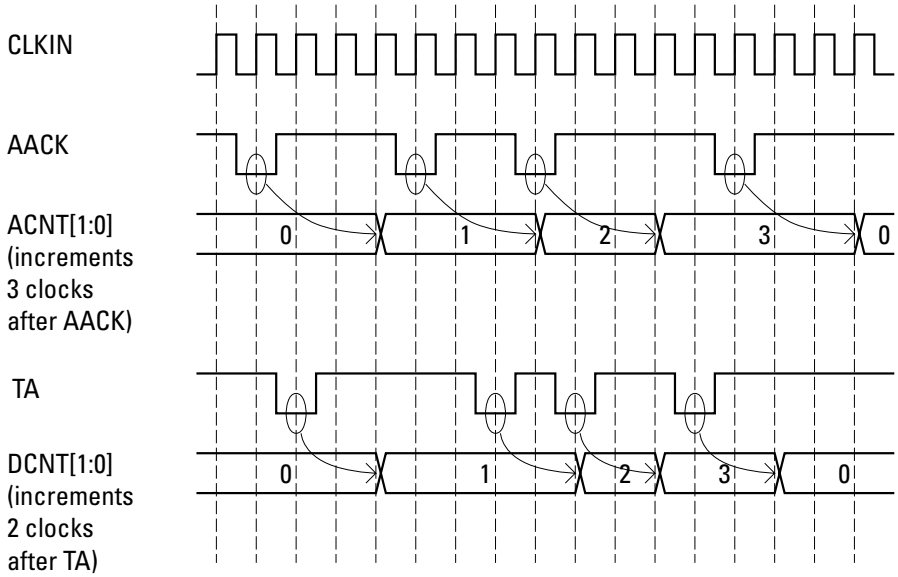
Signal	MPC8260 Pin	Analysis Probe DIP Switch	Equivalent Load (includes logic analyzer)
TCK* TMS* TRST*	AG5 AJ3 AH4	S1 = OFF	
		S1 = ON	
SRESET*	AF6	N/A	
HRESET*	AH5	N/A	

Signal	MPC8260 Pin	Analysis Probe DIP Switch	Equivalent Load (includes logic analyzer)
TT[0] TT[1] TT[2] TT[3] TT[4] AACK ARETRY TS TBST TA BG ABB APE NMI_OUT TEA DBB DBG	F1 G4 G3 G2 F2 F3 E1 E3 D3 C22 F4 E2 D1 T1 V5 V2 V1	N/A	
All other signals		N/A	

* Signal is on the JTAG port. The equivalent load shown does not include the emulation probe.

Theory of Operation

The analysis probe has a PLD that generates address and data counter signals that are used by the inverse assembler.



The address counter increments 3 clocks after the end of an address phase. The data counter increments 2 clocks after the end of a data phase.

Analysis Probe A probing solution connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer. Formerly called a “preprocessor.”

Background Debug Monitor Also called Debug Mode, In Background, and In Monitor. The normal processor execution is suspended and the processor waits for commands from the debug port. The debug port commands include the ability to read and write memory, read and write registers, set breakpoints and start the processor running (exit the Background Debug Monitor).

Debug Mode See *Background Debug Monitor*.

Debug Port A hardware interface designed into a microprocessor that allows developers to control microprocessor execution, set breakpoints, and access microprocessor registers or target system memory using a tool like the emulation probe.

Elastomeric Probe Adapter A connector that is fastened on top of a target microprocessor using a retainer and knurled nut. The conductive elastomer on the bottom of the probe adapter makes contact with pins of the target microprocessor and delivers their signals to connection points on top of the probe adapter.

Emulation Migration The hardware and software required to use an emulation probe with a new processor family.

Emulation Module (discontinued) An emulation module is installed within the mainframe of a logic analysis system. An E5901A emulation module is used with a *target interface module* (TIM) or an analysis probe. An E5901B emulation module is used with an E5900B *emulation probe* and does not use a TIM.

Emulation Probe An emulation probe is a standalone instrument connected via LAN to the mainframe of a logic analyzer or to a host computer. It provides run control within an emulation and analysis test setup. Formerly called a "processor probe" or "software probe."

Emulator An emulation module or an emulation probe.

Extender A part whose only function is to provide connections from one location to another. One or

more extenders might be stacked to raise a probe above a target microprocessor to avoid mechanical contact with other components installed close to the target microprocessor. Sometimes called a "connector board."

Flexible Adapter Two connection devices coupled with a flexible cable. Used for connecting probing hardware on the target microprocessor to the analysis probe.

Gateway Address An IP address entered in integer dot notation. The default gateway address is 0.0.0.0, which allows all connections on the local network or subnet. If connections are to be made across networks or subnets, this address must be set to the address of the gateway machine.

General-Purpose Flexible Adapter A cable assembly that connects the signals from an elastomeric probe adapter to an analysis probe. Normally, a male-to-male header or transition board makes the connections from the general-purpose flexible adapter to the analysis probe.

High-Density Adapter Cable A cable assembly that delivers signals from an analysis probe hardware interface to the logic analyzer pod cables. A high-density adapter cable has a single *MICTOR connector* that is installed into the analysis probe, and two cables that are connected to corresponding odd and even logic analyzer pod cables.

High-Density Termination Adapter Cable Same as a High-Density Adapter Cable, except it has a termination in the *MICTOR connector*.

In Background, In Monitor See *Background Debug Monitor*.

Inverse Assembler Software that displays captured bus activity as assembly language mnemonics. In addition, inverse assemblers may show execution history or decode control busses.

IP address Also called Internet Protocol address or Internet address. A 32-bit network address. It is usually represented as decimal numbers separated by periods; for example, 192.35.12.6.

Jumper Moveable direct electrical connection between two points.

JTAG (OnCE) port See *debug port*.

Label Labels are used to group and identify logic analyzer channels. A label consists of a name and an associated bit or group of bits.

Link-Level Address The unique address of the LAN interface. This value is set at the factory and cannot be changed. The link-level address of a particular piece of equipment is often printed on a label above the LAN connector. An example of a link-level address in hexadecimal: 0800090012AB. Also known as an LLA, Ethernet address, hardware address, physical address, or MAC address.

Mainframe Logic Analyzer A logic analyzer that resides on one or more board assemblies installed in a 16500, 1660-series, or 16600/700-series mainframe.

Male-to-male Header A board assembly that makes point-to-point connections between the female pins of a flexible adapter or transition board and the female pins of an analysis probe.

MICTOR Connector A high-density matched impedance connector manufactured by AMP Corporation. *High-density adapter cables* can be used to connect the logic analyzer to MICTOR connectors on the target system.

Monitor, In See *Background Debug Monitor*.

Pod A collection of logic analyzer channels associated with a single cable and connector.

Preprocessor See *Analysis Probe*.

Preprocessor Interface See *Analysis Probe*.

Probe Adapter See *Elastomeric Probe Adapter*.

Processor Probe See *Emulation Probe*.

Run Control Probe See *Emulation Probe* and *Emulation Module*.

Setup Assistant Wizard software program which guides a user through the process of connecting and configuring a logic analyzer to make measurements on a specific microprocessor. The setup assistant icon is located in the main system window.

Shunt Connector. See *Jumper*.

Solution A set of tools for debugging your target system. A solution

includes probing, inverse assembly, the B4620B Source Correlation Tool Set, and an emulation module.

Stand-Alone Logic Analyzer A standalone logic analyzer has a predefined set of hardware components which provide a specific set of capabilities. A standalone logic analyzer differs from a mainframe logic analyzer in that it does not offer card slots for installation of additional capabilities, and its specifications are not modified based upon selection from a set of optional hardware boards that may be installed within its frame.

State Analysis A mode of logic analysis in which the logic analyzer is configured to capture data synchronously with a clock signal in the target system.

Subnet Mask A subnet mask blocks out part of an IP address so the networking software can determine whether the destination host is on a local or remote network. It is usually represented as decimal numbers separated by periods; for example, 255.255.255.0.

Symbol Symbols represent patterns and ranges of values found on labeled sets of bits. Two kinds of symbols are available:

1) Object file symbols — Symbols from your source code, and symbols generated by your compiler. Object file symbols may represent global variables, functions, labels, and source line numbers.
2) User-defined symbols — Symbols you create.

Target Board Adapter A daughter board inside the E5900B emulation probe which customizes the emulation probe for a particular microprocessor family. The target board adapter provides an interface to the ribbon cable which connects to the debug port on the target system.

Target Control Port An 8-bit, TTL port on a logic analysis system that you can use to send signals to your target system. It does not function like a pattern generator or emulation module, but more like a remote control for the target's switches.

Target Interface Module A small circuit board which connects the 50-pin cable from an E5901A emulation module or E5900A emulation probe to signals from the debug port on a target system. Not used with the E5900B emulation probe.

TIM See *Target Interface Module*.

Timing Analysis A mode of logic

analysis in which the logic analyzer is configured to capture data at a rate determined by an internal sample rate clock, asynchronous to signals in the target system.

Transition Board A board assembly that obtains signals connected to one side and rearranges them in a different order for delivery at the other side of the board.

Trigger Specification A set of conditions that must be true before the instrument triggers. See the printed or online documentation of your logic analyzer for details.

1/4-Flexible Adapter An adapter that obtains one-quarter of the signals from an elastomeric probe adapter (one side of a target microprocessor) and makes them available for probing.

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Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

• Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.

• Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.

• If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.

• Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.

• Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

• Do not install substitute parts or perform any unauthorized modification to the instrument.

• Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

• Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

• Do not use the instrument in a manner not specified by the manufacturer.

To clean the instrument

If the instrument requires cleaning: (1) Remove power from the instrument. (2) Clean the external surfaces of the instrument with a soft cloth dampened with a mixture of mild detergent and water. (3) Make sure that the instrument is completely dry before reconnecting it to a power source.

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product..

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

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